A MINIATURIZED BRAIN-MACHINE-SPINAL CORD INTERFACE (BMSI) FOR CLOSED-LOOP INTRASPINAL MICROSTIMULATION

by

SHAHABEDIN SHAHDOOSTFARD

Submitted in partial fulfillment of the requirements for the degree of

Doctor of Philosophy

Thesis Advisor: Professor Pedram Mohseni

Department of Electrical Engineering and Computer Science

CASE WESTERN RESERVE UNIVERSITY

January 2018

CASE WESTERN RESERVE UNIVERSITY

SCHOOL OF GRADUATE STUDIES

We hereby approve the thesis/dissertation of

Shahabedin Shahdoostfard

candidate for the degree of Doctor of Philosophy*.

Committee Chair

Pedram Mohseni

Committee Member

Francis L. Merat

Committee Member

Soumyajit Mandal

Committee Member

Randolph J. Nudo

Date of Defense

July 06, 2016

*We also certify that written approval has been obtained

for any proprietary material contained therein.

© Shahabedin Shahdoostfard 2018
All Rights Reserved

This dissertation is dedicated to
my father, my mom, and my brother

NASER & AZAM & SHAYAN

Table of Contents

List of Tables

List of Figures

Acknowledgement

I would like to express my sincere gratitude and appreciation to my research advisor, Prof. Pedram Mohseni for his inspiration, guidance, mentorship, and full support throughout my Ph.D. study at Case Western Reserve University. This research work would not have been possible without his endless effort, extreme accuracy and enthusiastic dedication. I would also like to express my appreciation to my thesis committees, Prof. Randolph J. Nudo, Prof. Francis L. Merat, and Prof. Soumyajit Mandal for their participation, invaluable advice, thoughtful comments and suggestions to increase the quality of this research work.

I would also like to thank my previous and current colleagues in our research group, Bardia, Nok, Ali, Mehran, Mike, Debnath, Reza, Fatemeh, Hossein and from other research groups, Steve, for his help, useful discussions and technical support throughout the years. I should also acknowledge the hard work and contributions of my friends and colleagues in Prof. Nudo's lab at Kansas University Medical Center, Shawn, Scott, David, Stacey, Caleb, and Jordan in conducting biological experiments.

This work was supported by a generous gift from Ronald D. Deffenbaugh Foundation.

Finally, my profound gratitude goes to my family Azam, Naser, and Shayan. I have an amazing family, unique in many ways, and the stereotype of a perfect family in many others. Their support has been unconditional all these years; they have given up many things for me to be on the right track; cherished with me every great moment and supported me whenever I needed it.

A Miniaturized Brain-Machine-Spinal Cord Interface (BMSI) for Closed-Loop Intraspinal Microstimulation

Abstract

by

SHAHABEDIN SHAHDOOSTFARD

This project has developed two integrated microsystems fabricated in a 0.35-µm two-poly four-metal CMOS process for closed-loop intraspinal microstimulation (ISMS) controlled by intracortical neural spike activity for functional recovery after spinal cord injury (SCI). In particular, first, a system-on-chip (SoC) has been developed for robust neural recording of intracortical activity in the motor cortex region of the brain, and intraspinal microstimulation of spinal cord below the injury level, both *in vivo*. This SoC uniquely integrated two recording channels in the front-end featuring a band-pass frequency response in the range of 0.2-460 Hz for low-cutoff and 5-12 kHz for high-cutoff frequencies with total input noise voltage of 3.1µV_{rms} and noise efficiency factor (NEF) of 2.47, and four stimulating channels in the back-end for delivering charge balanced asymmetric biphasic or monophasic current pulses with passive discharge with output impedance of >100MΩ to the spinal cord.

Next, the second SoC has been developed as a *first ever* miniaturized Brain-Machine-Spinal Cord Interface (BMSI) for cortical control of ISMS based on the level of spike activity *in vivo*. The fabricated SoC incorporated two identical four-channel

modules, each compromising four neural recording channels, a DSP unit for on-the-fly stimulus trigger generation, and four stimulating channels for ISMS. The 3.46 × 3.46 mm^2 BMSI device also integrates a clock generator circuitry and radio frequency frequency-shift-keying (RF-FSK) transmitter for autonomous operation as a stand-alone system. The DSP unit of BMSI generates stimulus triggering based on the level of spike activity on the recording channels with different patterns and controls the ISMS with programmable delay from the last discriminated spike to mimic the natural time-delay existing in the nervous system. Measured results from benchtop testing, in vitro analysis, and biological experiments with anesthetized spinal cord injured rats are presented.

Chapter 1

Introduction

The goal of this Ph.D. research work is to develop a Brain-Machine-Spinal Cord Interface (BMSI) system-on-chip (SoC) for cortical control of intraspinal microstimulation. In particular, the major focus of this research is to integrate neural recording, digital signal processing (DSP), and intraspinal microstimulation (ISMS) on a single chip for long term functional recovery after spinal cord injury (SCI) by conducting experiments *in vivo*.

1.1 Background and Motivation

Approximately 6 million people in the United States are currently living with paralysis in which 23% of the cases are related to spinal cord injury (SCI) with significant lifetime costs incurred (e.g., ranging from ~$700K to >$3M for a 25-year old SCI patient) [1.1]. Hence, research is being performed worldwide to find solutions for repairing injured spinal cords and returning function and mobility to the SCI patients for augmented quality of life [1.2]-[1.5].

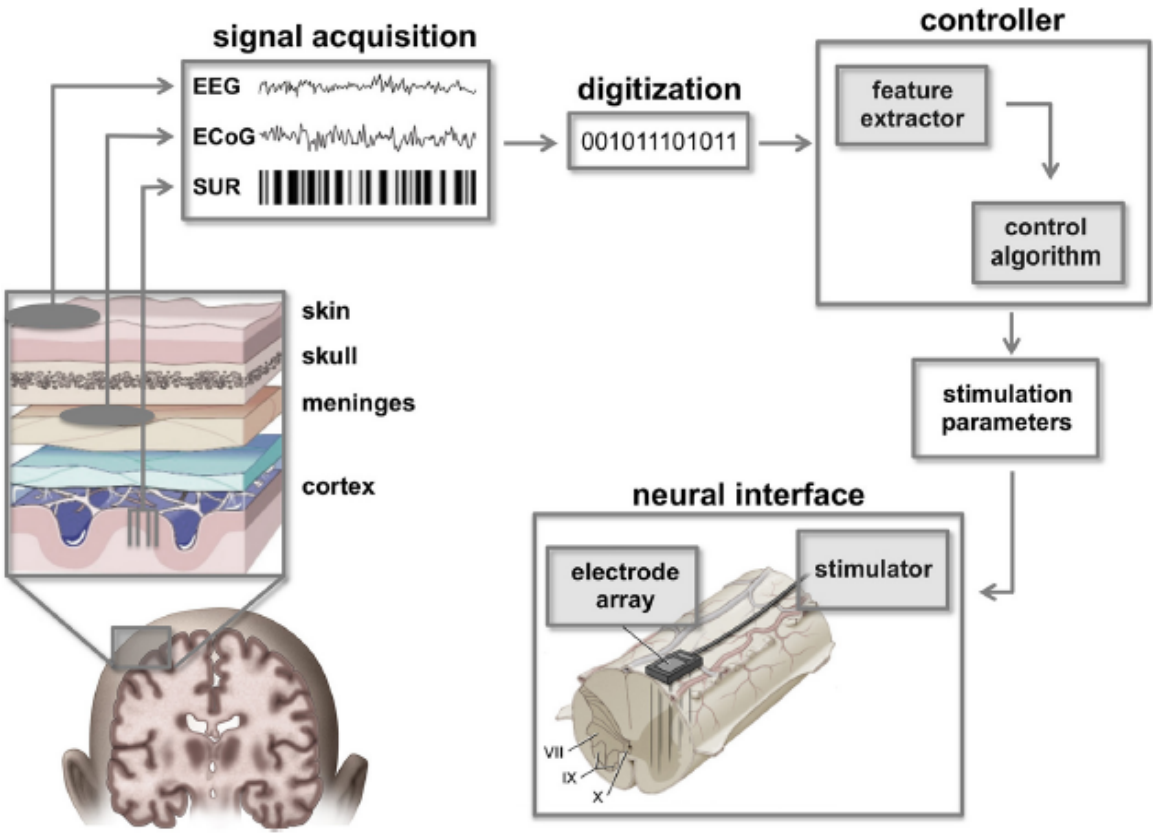

Figure 1.1: Conceptual illustration of a brain-machine-body interface (BMBI) [1.9]

Closed-loop neural interfaces have been shown to induce functional reorganization in both intact [1.6] and injured [1.7] nervous systems. These neuro-prosthetic devices, also known as brain-machine-body interfaces (BMBIs), as conceptually shown in Fig. 1.1, have evolved in the past several decades from simple, single-channel, wired devices to multifunctional, multichannel, wireless, closed-loop systems that are capable of bidirectional interfacing with the nervous system. Indeed, novel methodologies in low-power, low-noise integrated circuit (IC) design coupled with advancements in micro-electro-mechanical system (MEMS) technology have ushered in a new generation of implantable neuro-prostheses that aim to combine neural recording,

neural signal processing, and microstimulation functions in a single device for closed-loop operation [1.8].

Most BMBIs operate in a so-called control-mode paradigm in which the user's intent to produce voluntary control of the user's own body (or an external device in the case of a brain machine interface (BMI)) is detected in cortical activity, and, after processing, activates the target to produce an action [1.9]. While control-mode BMBIs are promising, there are substantial challenges with regard to designing optimal signal-processing and control algorithms, as well as their efficient hardware realization, in particular in a miniaturized form, for real-time execution. Furthermore, control-mode BMBIs often require significant learning by the user, depending upon the complexity of the task, and need to be implanted throughout the user's lifetime, facing additional challenges related to long-term feasibility.

An alternative, conditioning-mode approach for BMBIs is based on mechanisms underlying neuroplasticity. The ability of the nervous system to alter the strength of synaptic efficacy underlies learning and memory in healthy organisms, and is a mechanism for recovery after injury as well [1.7]. Using the same cortical command signals of control-mode BMBIs, it is possible to condition neural connections that are remote from each other by timing the application of a small electrical pulse in the target region so that it occurs after a natural delay following cortical spike activity.

Hence one promising approach employs an activity-dependent stimulation (ADS) paradigm in which artificial connections in the nervous system are created by converting neural activity recorded from one cortical area to electrical stimuli delivered to another cortical area [1.7], muscles [1.10], or spinal cord [1.11] in real time.

In a spinal cord injury that is caused by trauma to the spine, the nerve axons that carry sensory-motor signals back and forth between the brain and the rest of the body are damaged, while the neural circuits above and below the lesion generally remain intact. This provides an opportunity for cortical control of intraspinal microstimulation (ISMS) below the level of the lesion to bridge the damaged corticospinal pathways, re-establish the lost communication channels between the cerebral cortex and the spinal cord, and facilitate functional recovery after SCI [1.12].

Such an approach would require developing a corticospinal interface integrated circuit (IC) capable of low-noise intracortical spike recording and ISMS, as well as including appropriate signal-processing algorithms (and hardware-efficient architectures for their real-time implementation) for the transformation between the cortically recorded data and stimulation parameters, which is the focus of this PhD research work.

1.2 Neural Interface Systems: Previous Work

In this section, a review of the previous works in terms of efficacy of spinal cord stimulation and also developing neuro-prostheses for spinal cord injury is presented.

Great strides have been made to show evidence for benefits of electrical stimulation after spinal cord injury. Stimulation within the spinal cord activates local spinal networks in specific patterns to evoke functional movements. In an extensive work, Mushahwar et al. [1.13]-[1.15] demonstrated the ability of ISMS within the lumbar spinal cord to evoke standing and stepping movements. Building on top of that, Moritz et al. [1.16] have demonstrated that fore-limb movements can also be evoked by ISMS delivered to the cervical spinal cord in non-human primates.

More recently Sunshine et al. [1.17] have explored the fore limb movements evoked by cervical ISMS both before and after injury in a clinically-relevant rodent model of mid-cervical contusion injury. A wide variety of somatotopically organized fore limb movements could be evoked prior to injury from throughout the cervical spinal cord. Following injury, there was a transient period lasting approximately 3 weeks where movement variety was dramatically reduced. By 6 and 9 weeks after injury, however, a variety of movements could again be evoked via cervical ISMS, which were not statistically different from the effects prior to injury.

To show the effectiveness of electrical stimulation of spinal cord for motor function improvements, Edgerton et al. [1.18] applied electrical stimulation to the epidural surface of the spinal cord showing great promise for directly improving motor function after SCI. Epidural stimulation of the lumbar spinal cord can facilitate stepping movements after complete spinal transection, especially when combined with serotonin agonists and movement of a motorized treadmill underfoot. Besides, Brand et al. [1.19] showed when epidural stimulation combined with robotic assistance and motor training over complex surfaces; it also appears to facilitate the formation of a relay circuit by passing a complex, staggered lesion in animal models.

To show the importance of persistent of electrical stimulation after injury, Brus Ramer et al. [1.20] showed that electrical stimulation applied to the cortex or brainstem after selective SCI promotes axon sprouting and improves motor function persisting beyond the period of stimulation.

In terms of neuro-prosthesis for patients with SCI, although devices that have the capability of some sort of recording, microstimulation, or limited signal processing

functions, or a combination of them, have been previously developed for treating medically intractable epilepsy [1.21], [1-22], functional recovery after brain injury [1.23], [1.24], and deep brain stimulation treatment of Parkinson disease (PD) [1.25], [1.26], however a conditioning mode, miniaturized, and closed loop device has not been reported for spinal cord injury patients. Most of the mentioned devices were simple stimulators working in an open-loop fashion, e.g. PD devices. The other category of those devices have limited numbers of recording and stimulating channels while providing limited signal processing options which were basically a one to one recording to stimulation pairing scenario [1.24]. Also we have devices used for control mode recovery after SCI [1.11], which because of complicated algorithms and learning processes are not feasible for miniaturization and usually use desktop computers for their approaches.

A popular device that has been used for SCI-related experiments [1.27], [1.28] is a so-called Neurochip-II device first introduced by Stavros Zanos et al [1.29] as shown in Fig. 1.2.

Figure 1.2: Neurochip-II device inside the titanium casing [1.29].

This is a second generation of Nuerochip-I already introduced by the same group few years earlier [1.30]. Neurochip-2 device is made from commercially of the shelf (COTS) components and has two versions. Both versions have three recording and stimulation channels. The larger version, high output current version, has stimulation compliance voltage of ±50V, while the smaller version has stimulation compliance voltage of ±15V. The dimension of the smaller version is 63×63×30 mm^3. Reported power consumption is 420 mW for the period of simultaneous recording and stimulating task and operation can last for maximum of 48 hours with a two-battery pack. This device is too big and too power hungry to be considered for any possible future implantable applications. Also, lack of wireless communication seems to be a great disadvantage of Neurochip-2. Besides, flexibility of the implemented algorithm is limited to single stimulation based on every single discriminated spike. Finally, in terms of stimulation pulses, no mechanism for draining accumulated charge in the stimulation site exists after biphasic stimulation.

1.3 Proposed Research

Based on the discussion presented in the previous sections, the goal of this Ph.D. research work is to develop conditioning-mode single-chip SoC for closed loop cortical control of intraspinal microstimulation *in vivo*. A conceptual illustration of such a miniaturized closed loop brain-machine-spinal cord interface is depicted in Fig. 1.3.

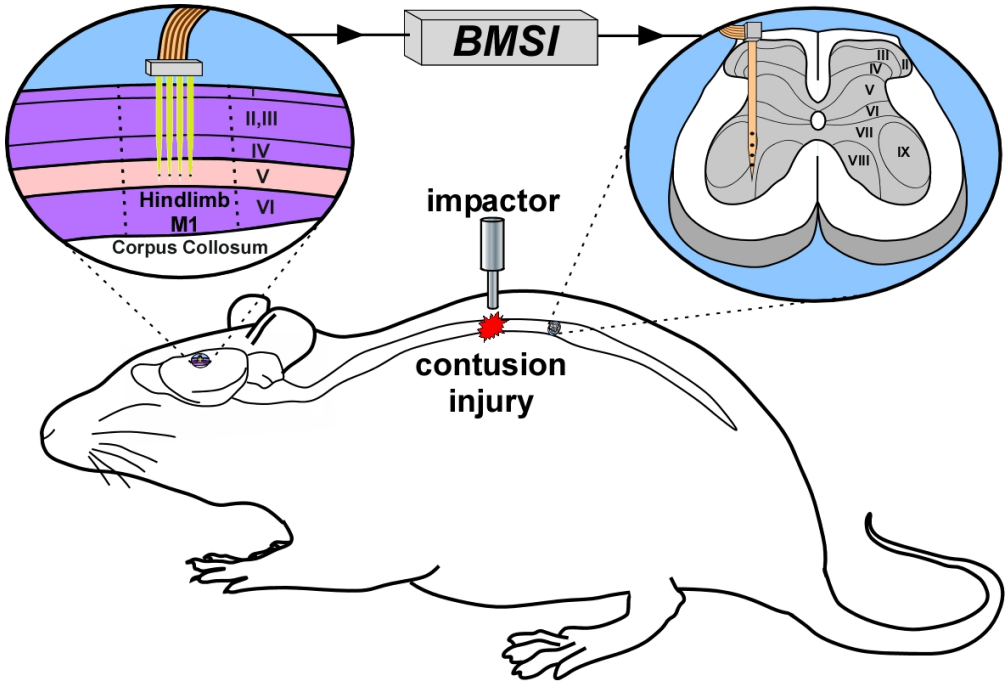

Figure 1.3: Conceptual illustration of our proposed brain-machine-spinal cord interface (BMSI); closed-loop intracortical control of intraspinal microstimulation (ISMS)

Throughout the course of this research project, two systems on chips (SoC) have been developed in 0.35-µm complementary metal-oxide-semiconductor (CMOS) technology, namely *SCI_Gen1* and *SCI_Gen2*. As an intermediate step between implementation of two SoCs, our proposed algorithm for the digital signal processing unit was first implemented on an FPGA and interfaced with first implemented chip (*SCI_Gen1*) to prove the functionality of the algorithm. In the final step, second chip was implemented, *SCI_Gen2*, which incorporated the expanded version of *SCI_Gen1* and integrated the proposed algorithm for an autonomous operation as a stand-alone system.

In particular, *SCI_Gen1* was developed for robust multichannel neural recording from motor cortex and intraspinal microstimulation on a single chip. *SCI_Gen1* incorporated two neural recording channels in the front-end and four electrical stimulation channels in the back end for generation of asymmetric biphasic current pulses

delivered to spinal cord. Electrical performances of the chip as well as *in vivo* functionality were verified for *SCI_Gen1*. Intracortical neural activity were recorded from cortex of an anesthetized rat and saved on a home-based computer for offline filtering and neural spikes discriminations. For verification of stimulating back end, EMG signals were recorded from hind limb muscles of the rat while *SCI_Gen1* was delivering current pulses to the spinal cord of the rat as a proof of effective intraspinal microstimulation.

Next, appropriate signal processing algorithms were developed on an FPGA platform for a meaningful translation from neural command signals to the ISMS pulses. In the proposed algorithm once a predetermined number of spikes are discriminated on each recording channel within pre-specified time bin duration, intraspinal microstimulation can occur based on any logic combination of those channels which have passed the criteria for spike activity. The proposed algorithm implemented on a Cyclone II FPGA device and interfaced with the *SCI_Gen1* device. Performance and functionality of the interfaced IC and FPGA are verified *in vivo* by real time neural recording, digital signal processing, and intraspinal microstimulation. Again, EMG signals were recorded to show the efficacy of ISMS in real time.

Finally, *SCI_Gen2* was developed which combines neural recording, digital signal processing (DSP), and ISMS in order to realize a closed loop brain machine spinal cord interface (BMSI) to improve the damaged corticospinal pathways, re-establish the lost communication channels between the cerebral cortex and the spinal cord, and facilitate functional recovery after SCI. For autonomous operation, new circuit blocks were also added to the *SCI_Gen2* device as a stand-alone BMSI system.

Table 1.1 summarizes target performance characteristics and biological test goals for the proposed microsystem in this research. The remainder of this thesis presents a detailed report on the design, development, and performance characterization of these microsystems as organized in the following chapters:

- Chapter 2 presents the *SCI_Gen1* SoC. The system design procedure for single-chip neural recording and microstimulating is described and measured results from benchtop electrical characterization and biological experiments with anesthetized rats are presented.

- Chapter 3 reports the field-programmable gate array (FPGA) implementation of a digital signal processing (DSP) unit for real-time generation of stimulus triggering from recorded neural activity. Measured results from benchtop and *in vitro* experiments as well as biological *in vivo* experiments on anesthetized rats by interfacing FPGA and *SCI_Gen1* SoC are presented.

- Chapter 4 combines our previous work in order to develop a BMSI SoC for closed-loop control of intraspinal microstimulation. Measured results from benchtop testing and biological experiments with anesthetized rats are presented.

- Chapter 5 draws final conclusions and highlights the major contributions of this research, as well as identifies further research opportunities in this field.

Table 1.1: Summary of Target Performance Characteristics

PERFORMANCE CHARACTERISTICS (BENCHTOP)		
SoC Functionality		Neural Recording, Digital Signal Processing, and Electrical Stimulation in a Closed-loop fashion
Number of Recording/Stimulating Channels		4/4
Power Supply		Recording Front-End and DSP Unit: 1.5V Stimulating Back-End (5V)
Recording Front-End For Intracortical Recording	Voltage Gain	50 – 66 dB
	ADC Resolution	Effective > 9 bits
	Input Noise Voltage	< $5\mu V_{rms}$
	Bandwidth	LCF: 0~500Hz HCF: 5~10kHz
Digital Signal Processing Unit	Functions	High pass filter, neural spike discriminator, stimulation pattern generator, neural recording blanking,
	Power Consumption	< 60μW
Stimulating Back-End for Intraspinal Microstimulation	Stimulus Waveform	Asymmetric Biphasic with passive discharge
	Output Current	0 – 100μA
	Stimulation Frequency	> 200 Hz
	Output Impedance	> 50MΩ
Other Functionalities		Wireless FSK Transmission (Uplink)
Technology		AMS 0.35μm CMOS
PERFORMANCE CHARACTERISTICS (*In Vivo*)		
Functionality Verification Phase w/ Anesthetized Rat	**Implantable SoC capable of real time** ▪ Multichannel neural recording from motor cortex ▪ Processing of Neural Data and generation of stimulus triggers ▪ Multichannel Stimulation of Spinal Cord ▪ Wirelessly sending out the on-chip data for clinical monitoring	

1.4 References for Chapter 1

[1.1] Christopher & Dana Reeve Foundation. Available online at www.christopherreeve.org.

[1.2] R. van den Brand, et al., "Restoring voluntary control of locomotion after paralyzing spinal cord injury," Science, vol. 336, pp. 1182-1185, June 1, 2012.

[1.3] Y. K. Lo, et al., "A 176-channel 0.5cm3 0.7g wireless implant for motor function recovery after spinal cord injury," in Dig. Tech. Papers IEEE Int. Solid-State Circuits Conf. (ISSCC'16), pp. 382-383, February 2016.

[1.4] L. R. Hochberg, et al., "Reach and grasp by people with tetraplegia using a neurally controlled robotic arm," Nature, vol. 485, pp. 372-375, May 2012.

[1.5] C. E. Bouton, et al., "Restoring cortical control of functional movement in a human with quadriplegia," Nature, vol. 533, pp. 247-250, May 2016.

[1.6] A. Jackson, J. Mavoori, and E. E. Fetz, "Long-term motor cortex plasticity induced by an electronic neural implant," Nature, vol. 444, pp. 56-60, 2006.

[1.7] D. J. Guggenmos, et al., "Restoration of function after brain damage using a neural prosthesis," Proc. Natl. Acad. Sci. USA (PNAS), vol. 110, no. 52, pp. 21177-21182, December 24, 2013.

[1.8] S. Stanslaski, et al., "Design and validation of a fully implantable, chronic, closed-loop neuromodulation device with concurrent sensing and stimulation," IEEE Trans. Neural Syst. Rehab. Eng., vol. 20, no. 4, pp. 410-421, July 2012.

[1.9] P. J. Grahn, et al., "Restoration of motor function following spinal cord injury via optimal control of intraspinal microstimulation: toward a next-generation closed-loop neural prosthesis," Front. Neurosci., vol. 8, no. 296, pp. 1-12, September 2014.

[1.10] C. T. Moritz, S. I. Perlmutter, and E. E. Fetz, "Direct control of paralyzed muscles by cortical neurons," Nature, vol. 456, pp. 639-643, 2008.

[1.11] J. B. Zimmermann and A. Jackson, "Closed-loop control of spinal cord stimulation to restore hand function after paralysis," Front. Neurosci., vol. 8, no. 87, pp. 1-8, May 2014.

[1.12] Mondello, S. E., Kasten, M. R., Horner, P. J., and Moritz, C. T., "Therapeutic intraspinal stimulation to generate activity and promote long-term recovery." Front. Neurosci. 8:21. doi: 10.3389/fnins.2014.00021, 2014.

[1.13] Mushahwar, V. K., and Horch, K. W. "Selective activation and graded recruit- ment of functional muscle groups through spinal cord stimulation." Ann. N.Y. Acad. Sci. 860, 531–535, 1998.

[1.14] Mushahwar, V. K., Gillard, D. M., Gauthier, M. J., and Prochazka, A. "Intraspinal micro stimulation generates locomotor-like and feedback- controlled movements." IEEE Trans. Neural Syst. Rehabil. Eng. 10, 68–81, 2002.

[1.15] Mushahwar, V. K., Aoyagi, Y., Stein, R. B., and Prochazka, A. “Movements generated by intraspinal microstimulation in the intermediate gray matter of the anesthetized, decerebrate, and spinal cat.” Can. J. Physiol. Pharmacol. 82, 702–714, 2004.

[1.16] Moritz, C. T., Lucas, T. H., Perlmutter, S. I., and Fetz, E. E. ”Forelimb movements and muscle responses evoked by microstimulation of cervical spinal cord in sedated monkeys.” J. Neurophysiol. 97, 110–120, 2007.

[1.17] Sunshine, M. D., Cho, F. S., Lockwood, D. R., Fechko, A. S., Kasten, M. R., and Moritz, C. T. “Cervical intraspinal microstimulation evokes robust forelimb movements before and after injury.” J. Neural Eng. 10:036001. doi: 10.1088/1741-2560/10/3/036001, 2013.

[1.18] Edgerton, V. R., and Harkema, S. “Epidural stimulation of the spinal cord in spinal cord injury: current status and future challenges. Expert Rev. Neurother. 11, 1351–1353. doi: 10.1586/ern.11.129, 2012.

[1.19] Van Den Brand, R., Heutschi, J., Barraud, Q., Digiovanna, J., Bartholdi, K., Huerlimann, M., et al. “Restoring voluntary control of locomotion after paralyzing spinal cord injury.” Science 336, 1182–1185. doi: 10.1126/sci- ence.1217416, 2012.

[1.20] Brus-Ramer, M., Carmel, J. B., Chakrabarty, S., and Martin, J. H. “Electrical stimulation of spared corticospinal axons augments connections with ipsi- lateral spinal motor circuits after injury.” J. Neurosci. 27, 13793–13801. doi: 10.1523/JNEUROSCI.3489-07, 2007.

[1.21] K. Abdelhalim, H. Mazhab Jafari, L. Kokarovtseva, J. L. P. Velazquez, and R. Genov, “64-channel UWB wireless neural vector analyzer SOC with a closed-loop phase synchrony-triggered neurostimulator,” IEEE J. Solid-State Circuits, vol. 48, no. 10, pp. 2494-2510, October 2013.

[1.22] T. L. Skarpaas and M. J. Morrell, “Intracranial stimulation therapy for epilepsy,” Neurotherapeutics, vol. 6, pp. 238-243, 2009.

[1.23] D. J. Guggenmos, M. Azin, S. Barbay, J. D. Mahnken, C. Dunham, P. Mohseni, and R. J. Nudo, “Restoration of function after brain damage using a neural prosthesis,” in Proc. Natl. Acad. Sci. USA, in press.

[1.24] M. Azin, D. J. Guggenmos, S. Barbay, R. J. Nudo, and P. Mohseni, “A battery-powered activity-dependent intracortical microstimulation IC for brain-machine-brain interface,” IEEE J. Solid-State Circuits, vol. 46, no. 4, pp. 731-745, April 2011.

[1.25] A. T. Avestruz, W. Santa, D. Carlson, R. Jensen, S. Stanslaski, A. Helfenstine, and T. Denison, “A 5μW/channel spectral analysis IC for chronic bidirectional brain-machine interfaces,” IEEE J. Solid-State Circuits, vol. 43, no. 12, pp. 3006-3024, December 2008.

[1.26] S. Stanslaski, P. Afshar, P. Cong, J. Giftakis, P. Stypulkowski, D. Carlson, D. Linde, D. Ullestad, A. T. Avestruz, and T. Denison, “Design and validation of a fully implantable, chronic, closed-loop neuromodulation device with concurrent sensing and stimulation,” IEEE Trans. Neural Syst. Rehab. Eng., vol. 20, no. 4, pp. 410-421, July 2012.

[1.27] Nishimura, Y., Perlmutter, S.I., & Fetz, E. E., “Restoration of upper limb movement via artificial corticospinal and musculospinal connections in a monkey with spinal cord injury.” Frontiers in neural circuits, 7, 2013.

[1.28] Nishimura Y, Perlmutter SI, Eaton RW, Fetz EE, “Spike-timing-dependent plasticity in primate corticospinal connections induced during free behavior.” Neuron 80(5):1301–1309, 2013.

[1.29] Zanos, S.; Richardson, A.G.; Shupe, L.; Miles, F.P.; Fetz, E.E., "The Neurochip-2: An Autonomous Head-Fixed Computer for Recording and Stimulating in Freely Behaving Monkeys," in Neural Systems and Rehabilitation Engineering, IEEE Transactions on , vol.19, no.4, pp.427-435, Aug. 2011.

[1.30] J. Mavoori et al., “An autonomous implantable computer for neural recording and stimulation in unrestrained primates,” J. Neurosci. Methods, vol. 148, no. 1, pp. 71–77, Oct. 2005.

Chapter 2

Integrated Microsystem for Intracortical Neural Recording and Intraspinal Microstimulation

This Chapter describes our *SCI_Gen1* system-on-chip (SoC) fabricated in AMS 0.35µm 2P/4M CMOS for reliably recording neural activity in the brain and delivering asymmetric biphasic current pulses as intraspinal microstimulation (ISMS) to the spinal cord *in vivo* as the first generation chip for functional recovery after SCI. The implemented SoC uniquely combines two neural recording in the front-end and four microstimulating channels in the back-end. In the following sections, system architecture of the neural recording and stimulating back end is described. Besides, measurement results of the bench-top characterization of the *SCI_Gen1* device as well as *in vivo* experiments conducted on anesthetized rats are presented [2.1]-[2.3].

2.1 System Architecture

Fig. 2.1 shows the IC architecture designed to interface with the cerebral cortex and the spinal cord via a pair of implanted microelectrode arrays. The IC incorporates two identical recording channels with digitally programmable gain and bandwidth for ac

amplification, dc baseline stabilization, high-pass filtering and 10b digitization of the recorded neural spikes. A 2:1 multiplexer and a data serializer block allow the user to access the digitized output of one channel in parallel or both channels in serial fashion, respectively. The IC also incorporates 4 identical stimulating channels to deliver ISMS trains of charge-balanced monophasic or asymmetric biphasic current pulses (0 to ~100µA) followed by passive discharge [2.4], [2.5].

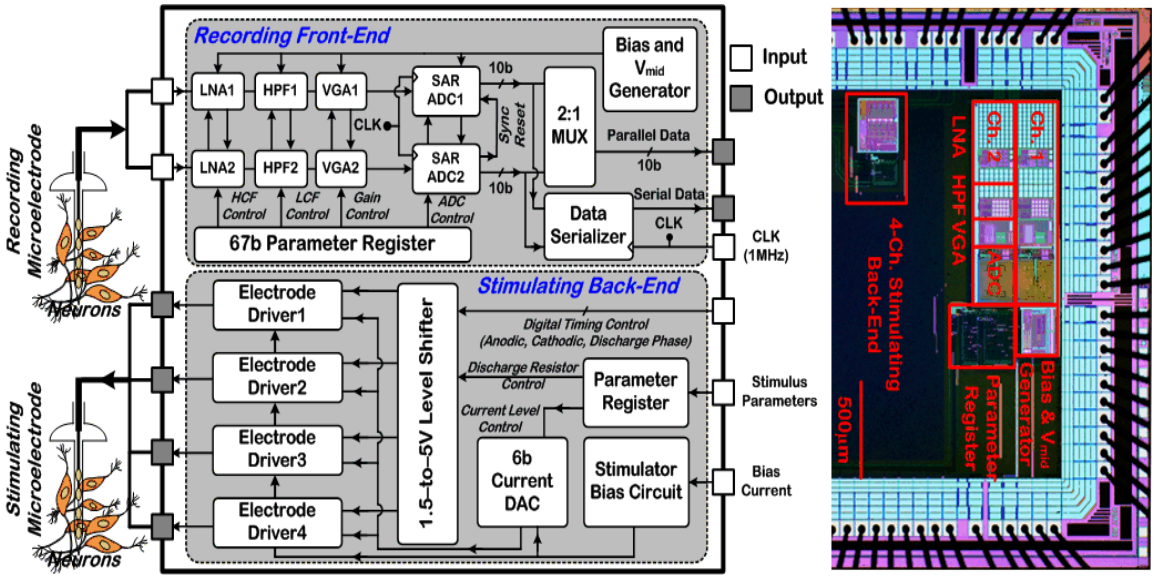

Figure 2.1: System architecture and die microphotograph of the *SCI_Gen1* fabricated in 0.35µm AMS 2P/4M CMOS technology.

In its nominal mode of operation for benchtop and *in vivo* testing purposes, the stimulating back-end is programmed to stimulate the spinal cord sequentially on all four channels with a programmable inter-channel delay to evoke four different limb movements in the subject. All current pulse parameters such as amplitude and duration as well as frequency and number within an ISMS train are also programmable for the IC.

2.2 Integrated Circuit Architecture

The system proposed in Fig. 2.1 has been realized using 0.35μm mix-mode CMOS process. Recording front-end was realized using thin-oxide transistors and operate at 1.5V whereas stimulating back-end was realized with thick-oxide transistors, usually used in IO cells, and operates at 5V. The following subsections describe designed circuitry for each individual block.

2.2.1. Recording Front-End

Fig. 2.2 depicts the circuit schematic of one channel in the recording front-end, operating from 1.5V and comprising a low-noise amplifier (LNA) with adjustable high cutoff frequency (HCF), high-pass filter (HPF) with adjustable low cutoff frequency (LCF), secondary amplifier with variable gain and adjustable offset, and 10b successive approximation register (SAR) ADC. The LNA provides fixed 32dB of ac gain via capacitive feedback, and dc baseline stabilization via a MOS-bipolar pseudo resistor in parallel with the feedback capacitor (0.7pF) [2.6]. An ultralow-transconductance operational transconductance amplifier (OTA) and a 16.7-pF capacitor form a 1^{st}-order HPF with an adjustable low cutoff frequency from 0 to 525 Hz by varying the OTA tail current. The analog HPF is designed to attenuate 60 Hz and remove low-frequency LFPs that might be present in the recorded neural data. The analog recording front-end features a bandpass frequency response with eight different gain values in 49 dB – 65.6 dB at 1kHz, as well as LCF and HCF values digitally programmable in 0.2 Hz – 460 Hz and 5 kHz – 11.9 kHz by tuning the bias currents of the HPF and LNA, respectively. The secondary amplifier with a resistive feedback provides additional 3-bit gain in the range

of 17-33.6 dB, and has a 4b offset adjustment mechanism by injecting a small dc current into the feedback path. The secondary amplifier provides a rail-to-rail output voltage swing and drives the 12-pF capacitor network of the subsequent ADC that converts the amplified neural data to a 10b digital code for further processing by the DSP unit [2.7].

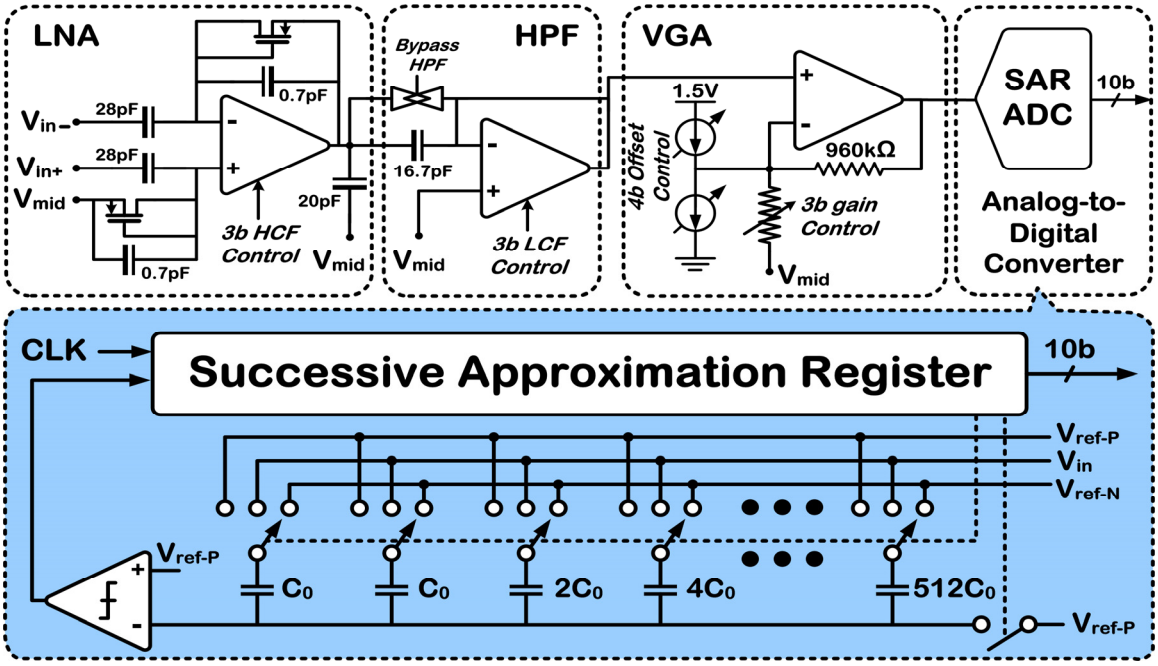

Figure 2.2: Circuit schematic of one channel in the recording front-end and the SAR ADC architecture.

The 10b SAR ADC, whose capacitive network is driven by the preceding variable-gain amplifier (VGA), is nominally clocked at 1MHz, with each ADC conversion cycle taking 28 clock cycles in which 16 cycles are dedicated to sampling, 1 cycle to hold, 10 cycles to approximation and 1 cycle to reset, thus providing a sampling frequency of 35.7kSa/s that is adequate for recording single-unit neural spikes with frequency components in 100Hz–10kHz. The extended sampling period helps relax current drive requirements of the preceding VGA for low-power operation. The ADC

digitizes the amplified/filtered neural data with a signal-to-noise and distortion ratio (SNDR) of 56dB (i.e., ENOB of 9b) at a maximum sampling frequency of 65kSa/s.

2.2.2. Stimulating Back-End

Fig. 2.3 shows the circuit schematic of the stimulating back-end, incorporating four identical electrode drivers that share a 6b current-based DAC. Each electrode driver operates from 5V and integrates a pair of pMOS (anodic) and nMOS (cathodic) current sources with thick-oxide transistors and boosted output impedance via negative feedback, provided by two op-amps ($A_{1,2}$), for constant-current stimulation [2.8]. The DAC operates from 1.5V and outputs a programmable current from 0 to 2.2μA with 6b resolution, which is then amplified to generate a maximum current of ~100μA for the anodic phase. The cathodic-phase current is set to be 1/3 of that in the anodic phase via proper transistor sizing ratios to generate an asymmetric biphasic current pulse for optimal use of available voltage headroom (5V). The DAC also employs a 4b current-adjust mechanism to fine tune the desired output stimulus current in the presence of process and voltage (PV) variations. Additional circuitry is used in each electrode driver to control the gate voltage of transistor M_3 in the nMOS current source and limit the drain-source voltage across $M_{2,3}$ to ~$V_{DD}/2$ (i.e., ~2.5V) for avoiding hot-carrier effects when the stimulus site voltage is near the supply rail [2.9]-[2.11].

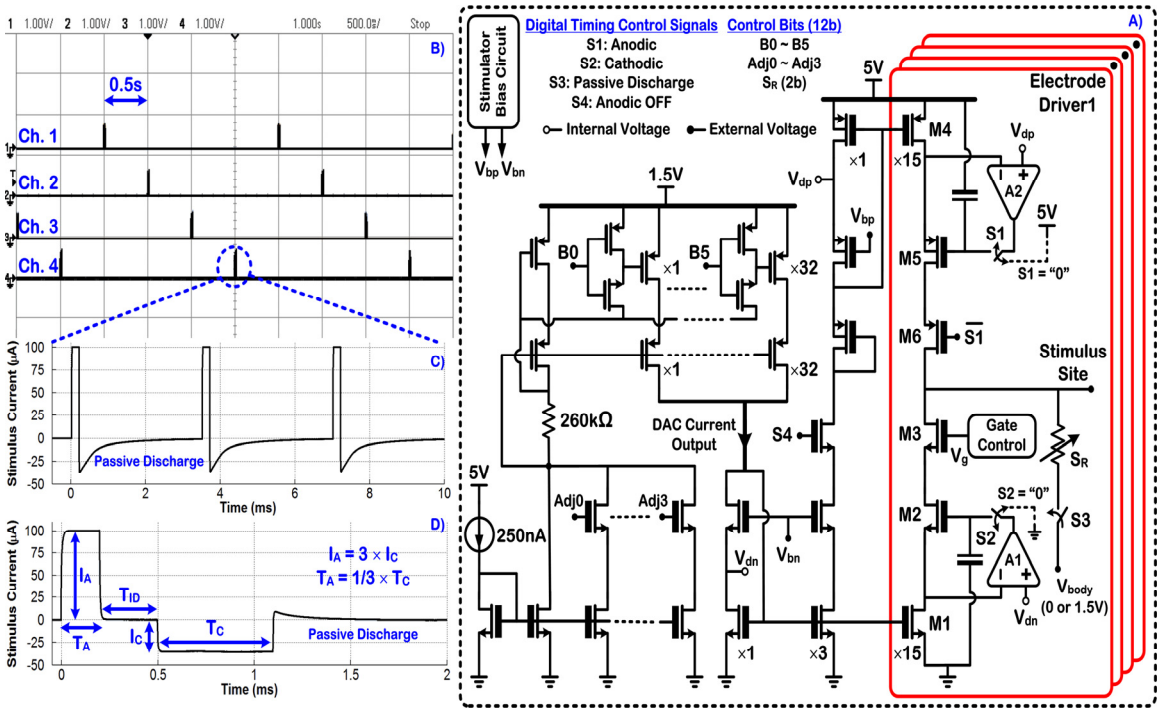

Figure 2.3: a) Circuit schematic of the stimulating back-end. b) Measured 4-channel sequential stimulation with a series resistive (1kΩ)-capacitive (20nF) load. c) Measured train of 3 monophasic current pulses with passive discharge used in sequential stimulation. d) Measured asymmetric biphasic current pulse.

2.3 Benchtop and *In Vivo* Measurement Results

A prototype SoC was fabricated in AMS 0.35μm 2P/4M CMOS, measuring ~2.9mm × 2.9 mm including the bonding pads (see Fig. 2.4). Electrical performance of individual circuit blocks was characterized in benchtop measurements, and their *in vivo* functionality was verified in biological experiments with anesthetized laboratory rats.

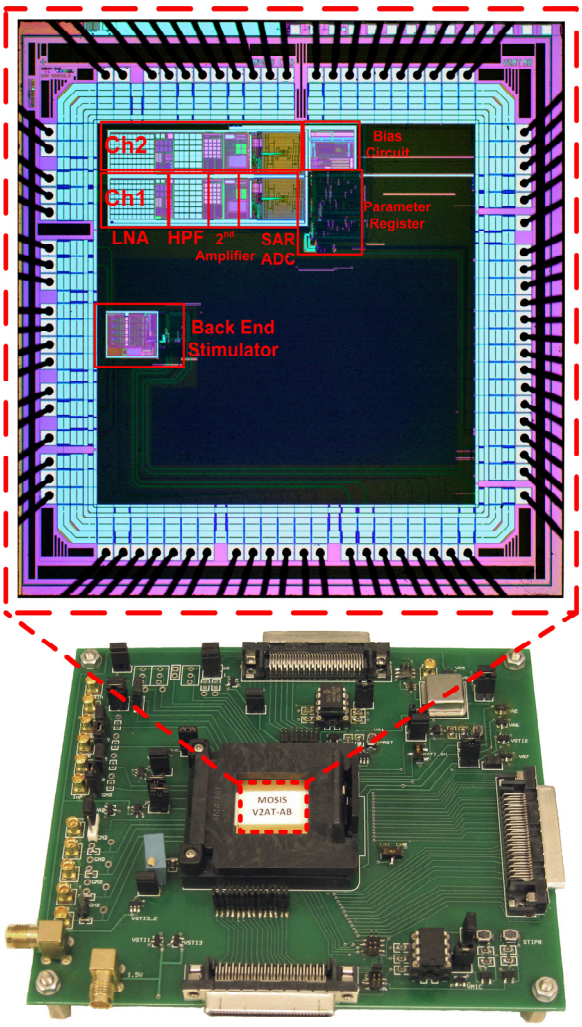

Figure 2.4: Top – Photograph of the custom PCB developed for biological tests and a die microphotograph of the 2.9 × 2.9 mm^2 SoC fabricated in AMS 0.35µm 2P/4M CMOS.

The top plots in Fig. 2.5 show the measured frequency response and input noise performance of the analog recording front-end. With the mid-band ac gain nominally set to 60dB and the LCF at 80Hz, the HCF could be varied from 5 to 11.9 kHz by changing the bias current of the LNA, as shown in the left plot. In the right plot, note how the HPF effectively removed the flicker noise contribution, when the LCF was digitally set to 272 and 397Hz (the HPF was bypassed for the case of the recording BW of 0.2Hz–11.9 kHz.) With the recording BW set to 272Hz–10kHz, the input-referred noise voltage measured

in 0.5Hz–50kHz was 3μVrms, leading to noise efficiency factor (NEF) of 2.47 for the LNA.

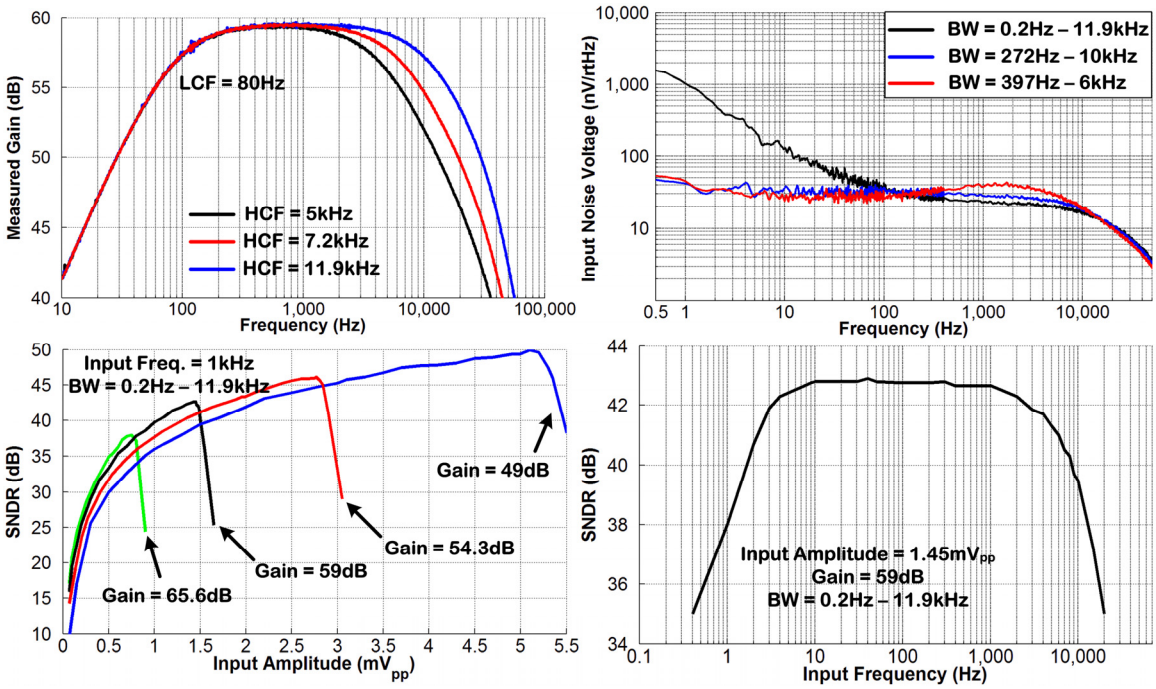

Figure 2.5: Top – Measured frequency response (left) and input noise (right) of the analog recording front-end. Bottom – Measured SNDR of the entire recording front-end vs. input amplitude (left) and frequency (right).

The bottom plots in Fig. 2.5 show the measured SNDR at the SAR ADC output versus the amplitude and frequency of a sinusoidal signal applied to the LNA input. The recording BW was digitally set to 0.2Hz–11.9 kHz. As can be seen in the left plot, lower gain values provided higher input dynamic range, whereas higher gain values provided better signal resolution. With a measured gain of 59dB, the recording front-end could provide peak SNDR of 42.6dB with input amplitude of 1.45mVpp at 1 kHz and >39.5dB within the frequency range of 100Hz – 10 kHz of extracellular neural spikes.

The top plots in Fig. 2.6 depict the measured stimulator output current versus its output voltage for four different DAC input codes when sourcing and sinking current in

the anodic and cathodic phases, respectively. The stimulator output voltage could reach at least 4.75V (going toward 5V) and 150mV (going toward 0V) when sourcing and sinking current, respectively, with a 5-V supply. The output impedance was measured to be >100MΩ (limited by the precision of our measurement setup), sufficiently high for constant-current stimulation.

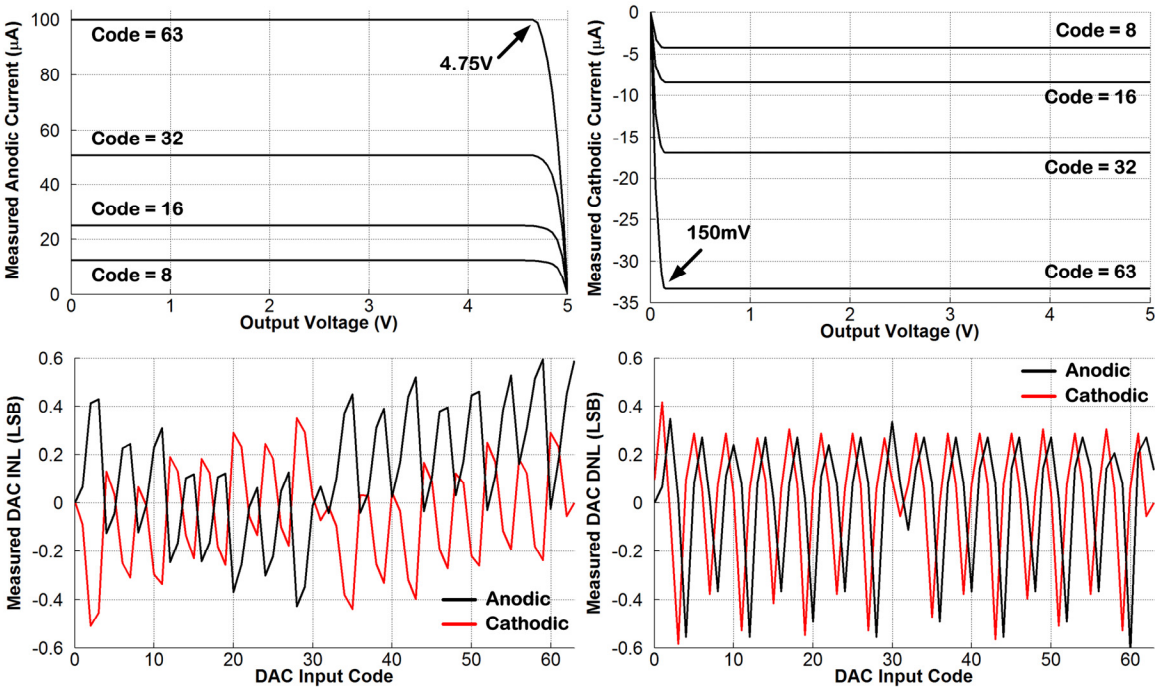

Figure 2.6: Top – Measured stimulator output current vs. output voltage in anodic (left) and cathodic (right) phases. Bottom – Measured DAC INL (left) and DNL (right) in both anodic and cathodic phases.

The bottom plots in Fig. 2.6 depict the current DAC INL and DNL that were measured to be less than ±0.62 LSB (anodic) and ±0.58 LSB (cathodic).

Table 2.1 tabulates measured performance of the recording and stimulating blocks of the IC.

Table 2.1: Summary of Measured Performance Characteristics for SCI_Gen1

<table>
<tr><th colspan="2">RECORDING FRONT-END</th><th colspan="3">STIMULATING BACK-END</th></tr>
<tr><td>AC Gain @ 1kHz</td><td>49 – 65.6dB</td><td></td><td>Anodic</td><td>Cathodic</td></tr>
<tr><td>HCF
LCF</td><td>5 – 11.9kHz
0.2 – 460Hz</td><td rowspan="2">Voltage Compliance (Max. I_{OUT})</td><td rowspan="2">4.75 (of 5V)</td><td rowspan="2">4.85 (of 5V)</td></tr>
<tr><td>Input Noise Voltage</td><td>$3\mu V_{rms}$
(0.5Hz – 50kHz)</td></tr>
<tr><td>NEF</td><td>2.47
(272Hz – 10kHz)</td><td>Max. I_{OUT}</td><td>100µA</td><td>33.3µA</td></tr>
<tr><td>CMRR/PSRR</td><td>56 / 63.4dB</td><td>Output Imp.</td><td colspan="2">> 100MΩ</td></tr>
<tr><td>INL/DNL</td><td>< ±1.15 LSB</td><td>INL (LSB)</td><td>< ±0.59</td><td>< ±0.50</td></tr>
<tr><td>SNDR/ENOB</td><td>56dB / 9b @ $f_{s,max}$ = 65kSa/s</td><td>DNL (LSB)</td><td>< ±0.62</td><td>< ±0.58</td></tr>
<tr><td rowspan="2">Power Dissipation</td><td rowspan="2">31.9µW
(0.2Hz – 11.9kHz;
f_{CLK} = 1MHz)</td><td>Supply Sensitivity</td><td>-69nA/V</td><td>-10nA/V</td></tr>
<tr><td>Current Efficiency</td><td>96.1%</td><td>94.7%</td></tr>
</table>

For *in vivo* tests, first a pair of recording and stimulating microelectrode arrays was acutely implanted in a healthy anesthetized rat's cerebral cortex and spinal cord respectively. Fig. 2.7 shows a 2-s window of recorded data from the rat's cerebral cortex and an expanded view of several extracellular neural spikes extracted from the data using offline spike discrimination. All amplitudes are shown as input-referred.

Next, the IC delivered 4-channel sequential stimulation with 1-s delay to the rat's spinal cord with a single monophasic current pulse (25µA, 200µs) followed by passive discharge. Stimulus site impedance was in the range of 50–60kΩ at 1kHz.

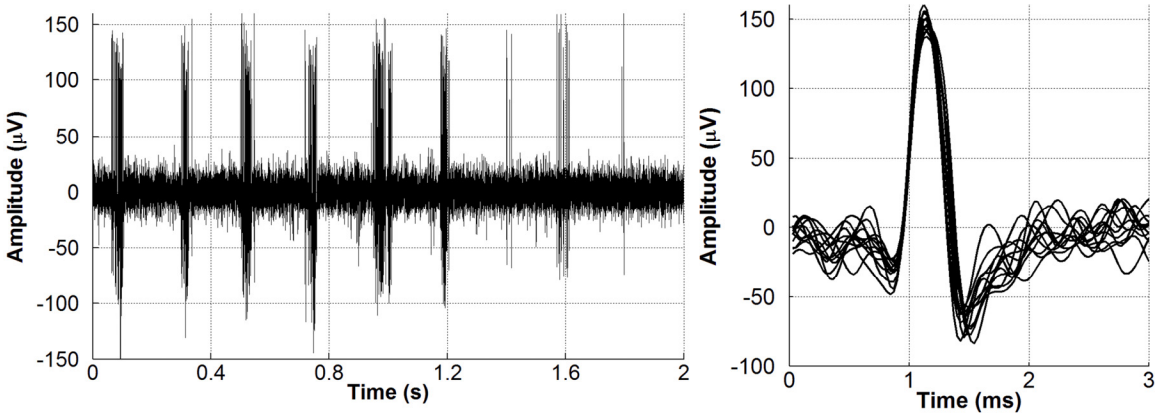

Figure 2.7: 2-second window of recorded data from the rat's cerebral cortex using the *SCI_Gen1* and an expanded view of 12 neural spikes discriminated offline.

Fig. 2.8 depicts the fine-wire electromyography (EMG) signals recorded with benchtop equipment from 3 muscles in the rat's hind limb (with the black bar showing the onset and duration of stimulus current pulse), demonstrating distinct muscle pattern activation via multichannel ISMS in the rat's spinal cord.

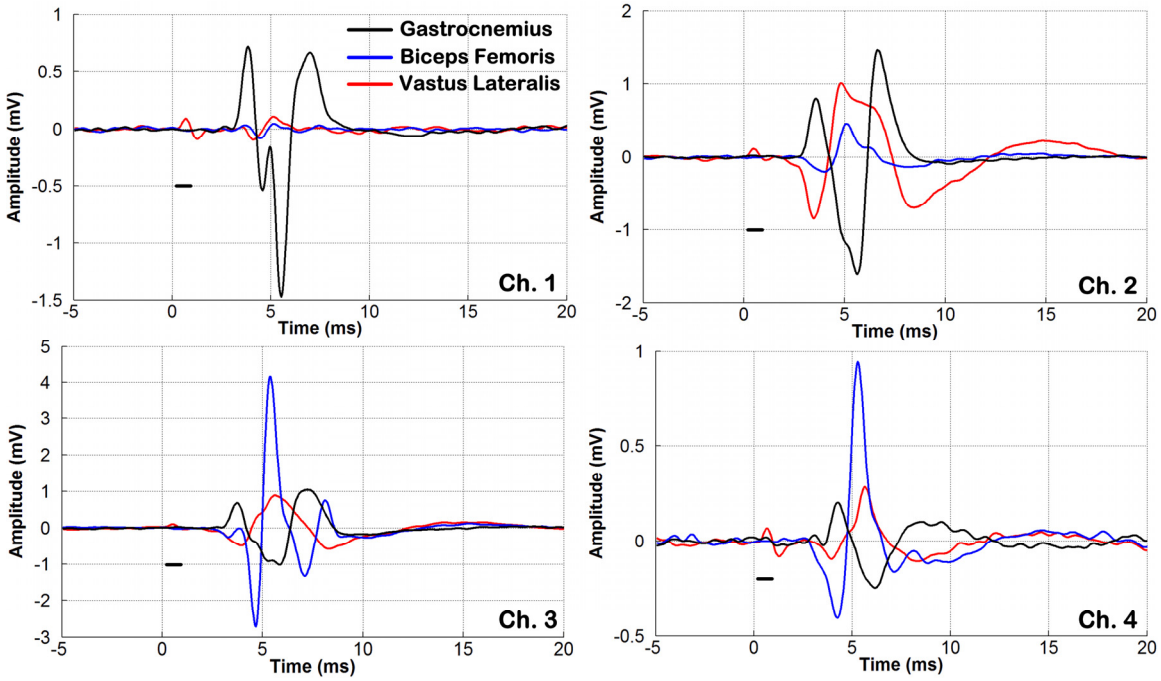

Figure 2.81: Recorded EMG signals from 3 hindlimb muscles activated via multichannel sequential ISMS in the rat's spinal cord using the *SCI_Gen1*.

In another *in vivo* experiment, same procedure was followed in a spinal cord injured (SCI) rat. For *in vivo* tests, a recording microelectrode array was acutely implanted in the sensory cortex of a ketamine-anesthetized rat. Fig. 2.9 shows a 1-second window of recorded data from the rat's cerebral cortex and an expanded view of several evoked neural spikes extracted from the data using offline spike discrimination. All amplitudes are shown as input-referred.

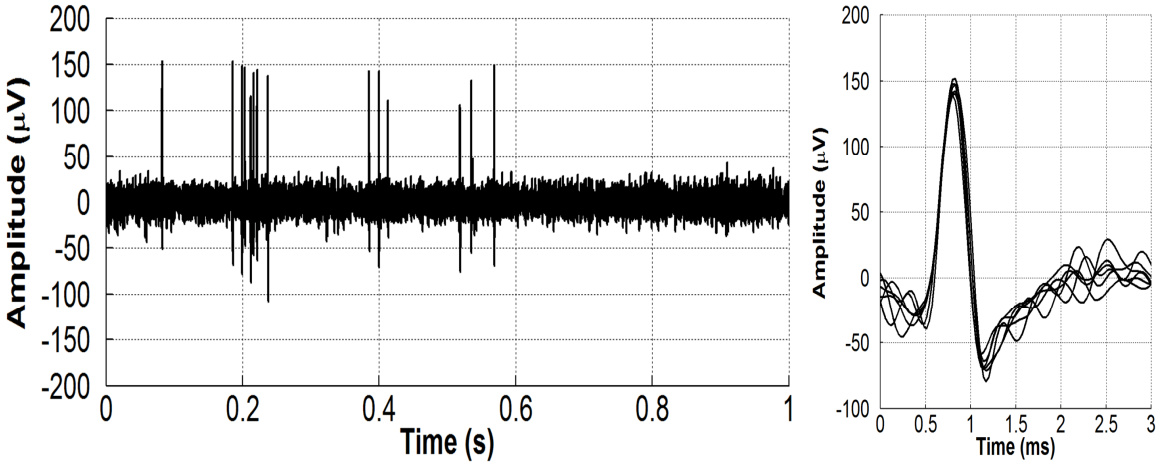

Figure 2.9: 1-second window of recorded data from the rat's cerebral cortex using the *SCI_Gen1* and an expanded view of six neural spikes discriminated offline.

Next, following the same procedure as previously described, a second rat was anesthetized with isoflurane and placed in a spinal stabilizer, and the thoracic and lumbar spinal column was exposed. This rat had also received a contusion injury to the thoracic spinal cord at level T8-T9 more than four weeks prior to the *in vivo* experiment.

Under ketamine anesthesia, a stimulating microelectrode array was acutely implanted in the rat's spinal cord below the level of the contusion injury, and the IC was used to deliver single-channel ISMS to the spinal cord with a single monophasic current pulse (anodic, 25μA, 200μs) followed by passive discharge.

Fig. 2.10 shows the fine-wire electromyography (EMG) signals recorded with benchtop equipment from two muscles in the rat's hindlimb (the horizontal black bar indicating the onset and duration of the stimulus current pulse), demonstrating successful muscle activation via ISMS in the SCI rat's spinal cord by the IC.

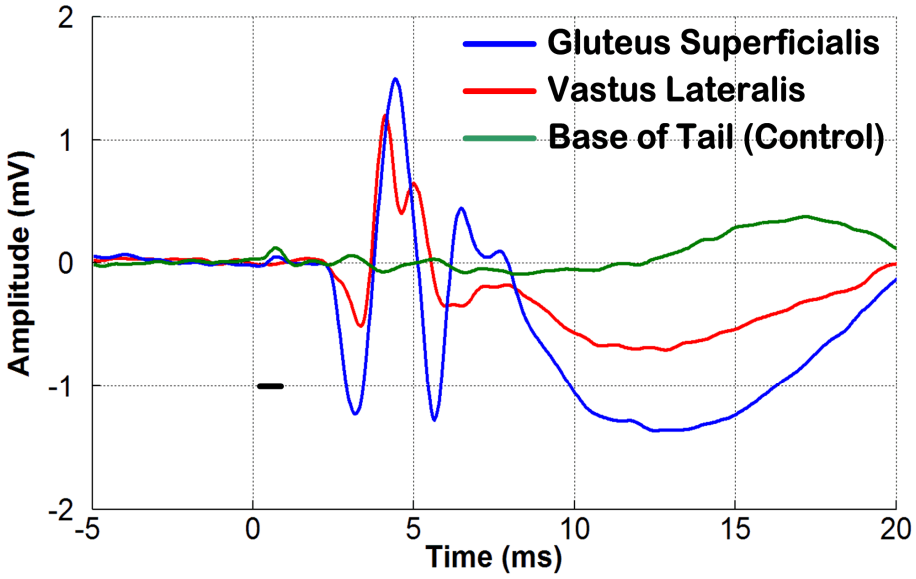

Figure 2.10: Recorded EMG signals from two hindlimb muscles of an SCI rat activated via ISMS in the rat's spinal cord using the *SCI_Gen1*. The horizontal black bar depicts the onset and duration of the single stimulus current pulse (monophasic anodic with passive discharge).

2.4 References for Chapter 2

[2.1] S. Shahdoost, S. Frost, R. Nudo, and P. Mohseni, "A multichannel corticospinal interface IC for intracortical spike recording and distinct muscle pattern activation via intraspinal microstimulation," in *Proc. 57th Annu. Int. IEEE Midwest Symp. Circuits and Systems (MWSCAS'14)*, pp. 310-313, College Station, TX, August 3-6, 2014.

[2.2] S. Shahdoost, S. Frost, , G. Van Acker, S. DeJong, C. Dunham, S. Barbay, R. Nudo, and P. Mohseni "Towards a miniaturized brain-machine-spinal cord interface (BMSI) for restoration of function after SCI," 41th Neural Interfaces Conference (NIC), June 23- 25, Dallas, Texas, 2014.

[2.3] M. Azin, D. J. Guggenmos, S. Barbay, R. J. Nudo, and P. Mohseni, "A battery-powered activity-dependent intracortical microstimulation IC for brain-machine-brain interface," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 731-745, April 2011.

[2.4] T. G. Constandinou, J. Georgiou, and C. Toumazou, "A partial-current-steering biphasic stimulation driver for vestibular prostheses," *IEEE Trans. Biomed. Circuits and Systems*, vol. 2, no. 2, pp. 106-113, June 2008.

[2.5] X. Liu, A. Demosthenous, and N. Donaldson, "An integrated implantable stimulator that is fail-safe without off-chip blocking capacitors," *IEEE Trans. Biomed. Circuits and Systems*, vol. 2, no. 3, pp. 231-244, September 2008.

[2.6] R. R. Harrison, "The design of integrated circuits to observe brain activity," *Proceedings of the IEEE*, vol. 96, no. 7, pp. 1203-1216, July 2008.

[2.7] M. D. Scott, B. E. Boser, and K. S. J. Pister, "An ultralow-energy ADC for smart dust," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1123-1129, July 2003.

[2.8] M. Ghovanloo and K. Najafi, "A compact large-voltage-compliance high-output-impedance programmable current source for implantable microstimulators," *IEEE Trans. Biomed. Eng.*, vol. 52, no. 1, pp. 97-105, January 2005.

[2.9] Y. Tsividis, *Operation and Modeling of the MOS Transistor*, 2nd ed., New York, NY: Oxford University Press, 1999.

[2.10] S. Guo, H. Lee, and P. Loizou, "A 9-bit configurable current source with enhanced output resistance for cochlear stimulators," in *Proc. Custom Integrat. Circ. Conf. (CICC'08)*, pp. 511-514, September 2008.

[2.11] M. M. Ahmadi, "A new modeling and optimization of gain-boosted cascode amplifier for high-speed and low-voltage applications," *IEEE Trans. Circuits and Systems-II*, vol. 53, no. 3, pp. 169-173, March 2006.

Chapter 3

FPGA Implementation of Stimulus Trigger Generation from Intracortical Spike Activity

This chapter describes required digital signal processing (DSP) for closed-loop cortical control of spinal cord stimulations as a new approach for restoration of functional recovery after spinal cord injury. In the following sections, we describe the developed algorithm by which recorded neural activity in the recording front-end of *SCI_Gen1* chip will control the electrical stimulation task of the stimulating back-end. The proposed DSP comprises a high-pass filter (HPF), spike discriminator unit, decision maker unit, and stimulator control unit as its core building blocks and includes auxiliary blocks for interfacing with *SCI_Gen1* device.

The proposed algorithm for the DSP unit has been implemented on a field-programmable gate array (FPGA), synthesized on to the Cyclone II FPGA, and interfaced with *SCI_Gen1* SoC [3.1]-[3.5]. Benchtop measurements and *in vivo* experiments results show the functionality and performance of the proposed algorithm in action.

In the following sections, first proposed algorithm is thoroughly described and then experimental results from interfacing FPGA implementation with *SCI_Gen1* chip are presented.

3.1 Operation Concept

Fig. 3.1 illustrates our strategy for generating stimulus triggers from intracortical neural spike activity recorded and discriminated in real-time from cortical motor regions [3.1]. For simplicity, a representative case involving two recording and four stimulating channels is depicted, although the general approach can be expanded to incorporate more recording and stimulating channels as well.

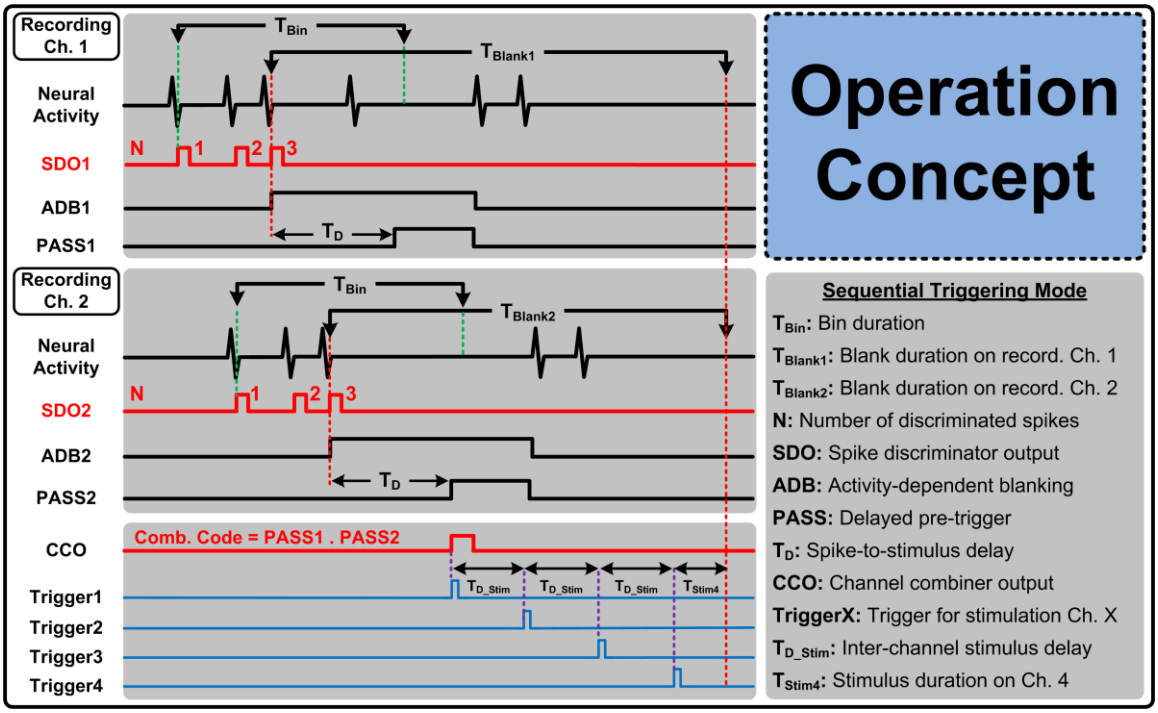

Figure 3.1: Conceptual illustration of the strategy for stimulus trigger generation from intracortical neural spike activity. A representative case involving two recording and four stimulating channels in sequential triggering mode is illustrated.

As seen in Fig. 3.1, a spike discriminator output signal, SDO, is activated on each recording channel upon successful discrimination of each neural spike event. Once a predetermined number of neural spikes, N, are discriminated on each recording channel within a pre-specified time bin duration, T_{Bin}, a PASS signal is activated on each channel after a programmable time delay, T_D, following the discrimination of the last spike. The trigger signals for stimulation activation are then generated based upon any logic combination of the PASS signals. For example, Fig. 3.1 illustrates a representative case when sequential triggering is generated once trigger-generation criteria are simultaneously satisfied on both input data channels (i.e., trigger generation is based upon the logic AND function of the two PASS signals).

Implemented in hardware using an FPGA, all parameters in Fig. 3.1 are user-adjustable within a pre-specified range that is guided by design considerations when the implementation is ultimately ported from the FPGA to an IC platform for full miniaturization of such BMSI systems.

While Fig. 3.1 depicts a four-channel, *sequential* triggering scenario with a programmable inter-channel delay, T_{D_Stim}, the reconfigurable FPGA-based realization also supports other triggering scenarios, e.g., *individual* triggering where each trigger signal itself (i.e., *TriggerX*) is defined as a logic combination of the *PASS* signals using a 4b combination code.

As seen in Fig. 3.1, the strategy also provides an ability to blank (i.e., disregard) the neural data on a recording channel during T_{Blank} (i.e., from discrimination of the last spike until the end of stimulus duration on all four channels). The rationale and

implementation details of blanking for both sequential and individual triggering cases are further explained in Blanking Section.

3.2 FPGA System Architecture

Fig. 3.2 depicts the system architecture and corresponding operation timing diagram for hardware realization of the stimulus trigger-generation strategy on an FPGA. The core building blocks of the system include a digital highpass filter (HPF), neural spike discriminator, and decision-making circuitry, whereas the auxiliary blocks include timing & data manager unit, data serializer, reset synchronizer, and a 219b latched shift register.

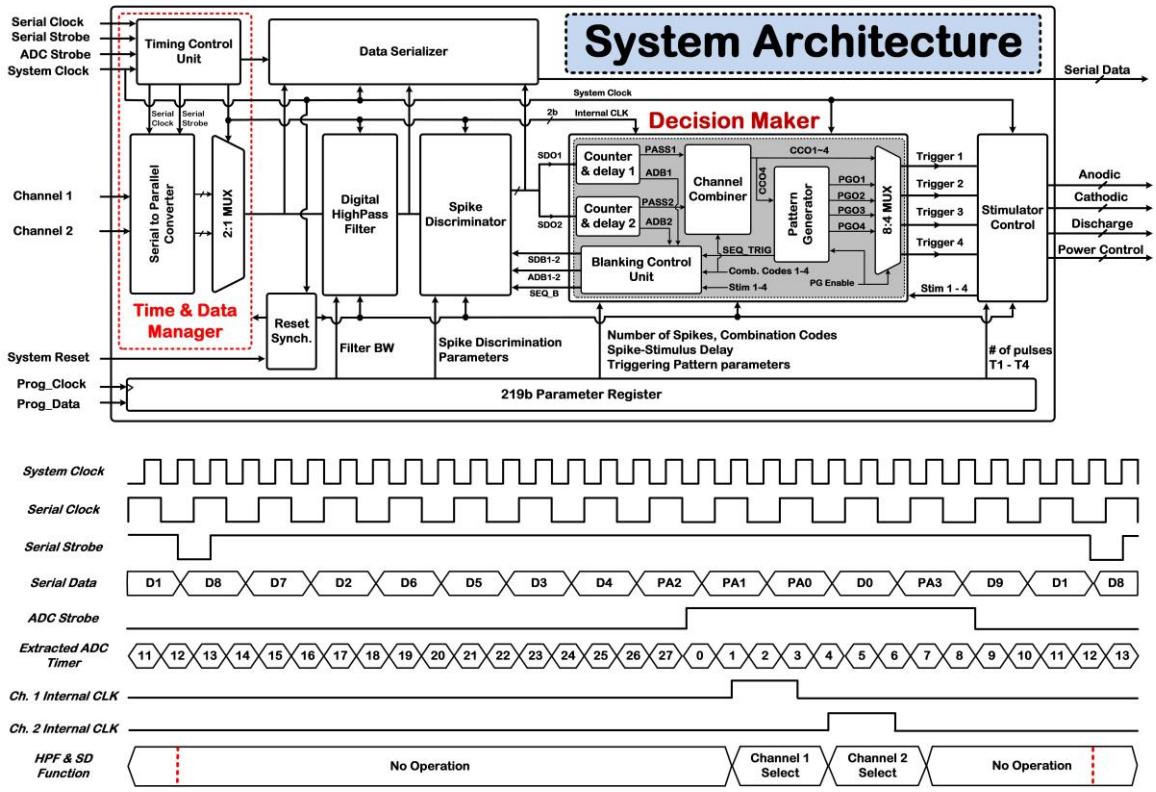

Figure 3.2: System architecture and timing diagram for hardware realization of the strategy for stimulus trigger generation from intracortical neural spike activity.

The embedded data serializer sends out the raw and filtered neural data as well as the *SDO* signal on each channel serially using an internally generated clock signal (500kHz) for external monitoring. The latched shift register provides all the programming and control bits for the FPGA operation. The other building blocks are described below in further detail.

3.2.1 Time and Data Manager

The timing & data manager unit interfaces with the spike-recording front-end circuitry to prepare the data on each channel for processing and to manage the timing of the FPGA operation. Specifically, the timing control unit of this block, which receives a 1MHz system clock along with serial clock and strobe signals from the recording front-end, extracts the timing information of the incoming serial data on each recording channel and manages the operation of a serial-to-parallel converter and a 2:1 multiplexer in order to convert the incoming serial data per channel into 10b parallel data for further processing by the FPGA.

To manage the timing of the FPGA operation, the timing control unit also generates two internal clock signals (for Ch. 1 and Ch. 2) that are utilized by the 2:1 multiplexer, digital HPF, spike discriminator, and decision maker. The latter also uses the 1MHz system clock for operation flexibility.

The operation timing diagram in Fig. 3.2 is illustrated based on the premise that each conversion cycle of the analog-to-digital converter (ADC) in the spike-recording front-end takes 28 cycles of the 1MHz system clock. This design strategy helps reduce

the power consumption per channel in the recording front-end, while still providing a sampling frequency of ~35.7kSa/s/ch.

As seen in Fig. 3.2, each of the two internal clock signals lasts for two cycles of the 1MHz system clock, with one additional clock cycle as delay between the two channels. Hence, the processing of each data channel takes only three system clock cycles, enabling the same architecture to simultaneously handle up to nine recording channels in any future expansion of the system functionality.

3.2.2 Digital High-Pass Filter

A 1st-order, infinite impulse response (IIR), digital HPF removes any residual dc offsets or low-frequency noise/artifacts from the multiplexed/digitized input neural data prior to online spike discrimination. As shown in Fig. 3.3, the HPF has direct form II architecture and a transfer function that can be expressed as:

$$H(z) = \frac{1 - z^{-1}}{1 - (1 - K)z^{-1}}, \tag{3.1}$$

where factor *K* is the user-set HPF coefficient that controls the filter bandwidth (BW). Specifically, factor *K* can be either 1/16 or 1/8, which results in a filter BW of 366Hz or 756Hz, respectively, from a 1MHz system clock. Moreover, the filter coefficients are judiciously selected to perform the filtering using arithmetic shifts, subtraction and addition only, obviating any need for digital multipliers or dividers.

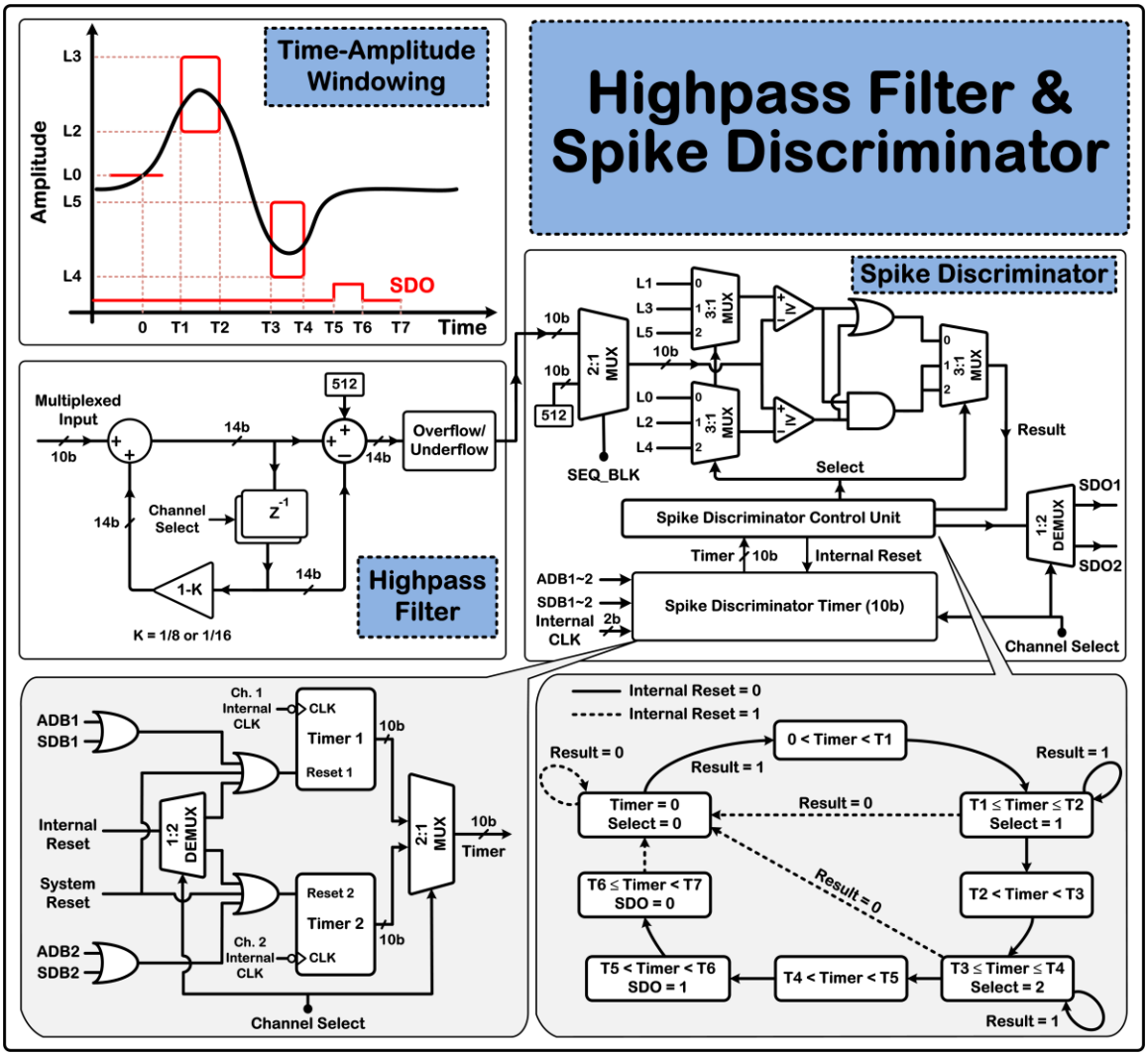

Figure 3.3: Detail presentation of high pass filter and spike discriminator blocks. Conceptual illustration of the time-amplitude window discriminator is shown on top left. Negative threshold level L_1 (not shown in bottom left) is used in the algorithm to discriminate waveforms with reverse polarity (i.e., negative-going initial portion), if necessary. The finite state machine (FSM) for spike discrimination algorithm is shown with illustration of timers and resets selection process, and the role of blanking related signals.

3.2.3. Neural Spike Discriminator

As shown in Fig. 3.3, the system employs thresholding and two user-adjustable time-amplitude windows for real-time neural spike discrimination from noise and other artifactual signals. Once the signal waveform crosses a user-defined threshold level, L_0,

the spike discriminator is activated to check whether the signal waveform subsequently passes through both time-amplitude windows (solid red boxes). If a spike event is accepted on any channel, the corresponding *SDO* signal is activated for the decision-making circuitry to generate the stimulus trigger signals, as described in further detail below. A negative threshold level, L_1 (not shown), is also used to discriminate waveforms with reverse polarity (i.e., negative-going initial portion). The timing parameters $T_{1\sim4}$ and $T_{5\sim7}$ can be user-set up to ~ 7.2ms and 28.6ms, respectively, in steps of 28μs.

Fig. 3.3 also depicts the finite-state machine (FSM) diagram of the control unit of the neural spike discriminator along with the architecture of its timer block. When each internal clock signal is active, the 10b timer information of the corresponding recording channel is selected and sent to the spike discriminator control unit. The timer information of each channel can be individually reset either internally or externally via the system reset signal, or via the blanking-related signals, *ADB* and *SDB*, as explained in further detail in dedicated Blanking Section.

3.2.4. Decision Maker Circuitry

The decision maker uses the *SDO* signals as input and, based upon various user-adjustable settings, generates the four trigger signals for either the individual or sequential stimulus-triggering scenario. Specifically, the counter & delay unit of this block counts a programmable number of discriminated neural spikes ($N \leq 15$) within a user-adjustable time bin duration, $T_{Bin} \leq$ ~0.5 second in steps of 56μs, and generates the *PASS* signal for each channel with a programmable delay, $T_D \leq$ ~28.6ms in steps of 28μs, following the discrimination of the last spike. The trigger signals are then generated

based upon the desired stimulus-triggering scenario, as selected by an 8:4 multiplexer at the output of the decision maker (see Fig. 3.2.)

In the individual triggering scenario, a channel combiner block, which is implemented as a programmable gate array, generates each trigger signal, *TriggerX*, independently as a logic combination of the two *PASS* signals using a 4b combination code that is unique for each stimulus channel. By de-activating the *PG_Enable* signal, the 8:4 multiplexer uses the four channel combiner outputs, *CCO1~4*, as the four trigger signals in this case.

In the sequential triggering scenario, the four output trigger signals are obtained from a pattern generator block and can be nominally generated with a programmable, constant inter-channel stimulus delay, $T_{D\_Stim} \leq$ ~1 second in steps of 56µs, as previously shown in Fig. 3.1. The pattern generator also supports another sequential triggering scenario in which simultaneous triggering occurs on the first two stimulus channels (*Trigger1,2*) followed by simultaneous triggering on the next two channels (*Trigger3,4*) after a delay of $3 \times T_{D\_Stim}$. It should be noted that simultaneous, 4-channel triggering can also be supported by simply setting T_{D_Stim} to zero.

By activating the *PG_Enable* signal, the 8:4 multiplexer uses the four pattern generator outputs, *PGO1~4*, as the four trigger signals in this case. Also, to provide savings in the number of programming and control bits for the FPGA operation, the pattern generator utilizes the same 4b combination code used for the stimulating channel 4 in the individual triggering scenario to define the neural input-based criteria for sequential triggering.

3.2.5. Reset Synchronizer

In this design, based on the requirement of each block or sub-block, both synchronous and asynchronous reset signals have been used. Synchronous resets usually do not have meta-stability problems because they always occur at the active edge of the clock for each flip-flop. But this is not the case for asynchronous resets.

The main problem with asynchronous resets is that they are asynchronous both at the assertion and at the de-assertion of the reset. The assertion is a not problematic, but the de-assertion is. If the asynchronous reset is released at or near the active clock edge of a flip-flop, the output of the flip-flop could go metastable and thus the reset state of the ASIC could be lost. To avoid this meta-stability issue for asynchronous reset signals, reset synchronizer is used to make sure asynchronous reset signals are de-asserted on the opposite edge of active clock for each specific flip-flop.

3.2.6. Stimulator Control

The stimulator control unit generates the requisite timing control signals for the stimulating back-end to control the anodic, cathodic, and passive discharge phases of the stimulus waveform. Asymmetric biphasic current pulse parameters such as duration of anodic phase, interphase delay, duration of cathodic phase, and duration of passive discharge as well as frequency and number of pulses within an ISMS train can be programmed for the BMSI via this block.

3.3. Blanking Schemes

As briefly mentioned in previous sections, our stimulus trigger-generation strategy also provides an ability to blank (i.e., disregard) the input neural data on some or even all of the recording channels for specific periods of time. There are two reasons behind the implementation of such blanking schemes. First, although the time-amplitude window discriminators (as opposed to simple spike thresholding) should be capable of discriminating neural spike waveforms from stimulus artifacts (by proper adjustment of parameters in the two windows), the blanking schemes further ensure that stimulus artifacts, if present in the BMBI system, will not lead to false-triggering.

Second, since neural spikes can occur asynchronously at any time during the BMBI system operation (e.g., during a period of stimulation), the blanking schemes provide a mechanism to prevent unwanted stimulus triggering during a period of stimulation, and to keep track of the trigger-generating spikes in any post hoc analysis of spike-stimulus pairs.

As seen in Fig. 3.2, the blanking schemes are implemented by a blanking control unit within the decision maker that provides additional inputs (ADB1~2, SDB1~2, SEQ_BLK) to the neural spike discriminator. Different blanking schemes are devised for individual and sequential triggering scenarios and described in further detail below.

3.3.1. Blanking Scheme for Individual Triggering

In an individual triggering scenario, each trigger signal itself (i.e., TriggerX) is defined as a logic combination of the PASS signals using a 4b combination code. As a representative case, Fig. 3.4 illustrates various signals and their relative timings that are

involved in blanking for individual triggering on stimulating channel 3, initiated when trigger-generation criteria are satisfied on the first input data channel only (i.e., Trigger3 is set to be PASS1 signal.) Once spike-discrimination criteria are satisfied on any recording channel, an activity-dependent blanking signal, ADB, is activated on that same channel that blanks its input data by resetting the timer information of the recording channel in the neural spike discriminator (see Fig. 3.3) Once the ADB signal is de-activated on the falling edge of the corresponding PASS signal, the recording channel is ready again to check the spike-discrimination criteria.

However, depending upon the user-set combination code to define TriggerX, only a subset of the recording channels might actually be involved in stimulus trigger generation in a given experiment (e.g., recording Ch. 1, but not Ch. 2, in Fig. 3.4). A second blanking signal, namely, stimulus-dependent blanking (SDB) is then employed to prolong the blanking duration only on those recording channels involved in trigger generation. Specifically, the blanking control unit incorporates a lookup table with the user-defined combination codes as its input in order to generate a series of static command signals, BlankXY, at the output. In conjunction with StimX signals, which indicate the duration of stimulation on channel X and are typically provided via the stimulator controller of the BMBI system, the two SDB signals are generated as shown in Fig. 3.4.

Specifically, in Fig. 3.4, Blank31 signal at the output of the lookup table, as well as Stim3 signal, will be active (all other BlankXY and StimX signals will be inactive), which will then activate the SDB1 signal only.

Hence, recording Ch. 1 (i.e., source of Trigger3) will continue to be blanked beyond ADB1 until stimulation on channel 3 is terminated, whereas recording Ch. 2 will not be blanked beyond ADB2. Similar to ADB signals, the SDB signals achieve blanking by resetting the timer information of the corresponding recording channels in the neural spike discriminator (see Fig. 3.3)

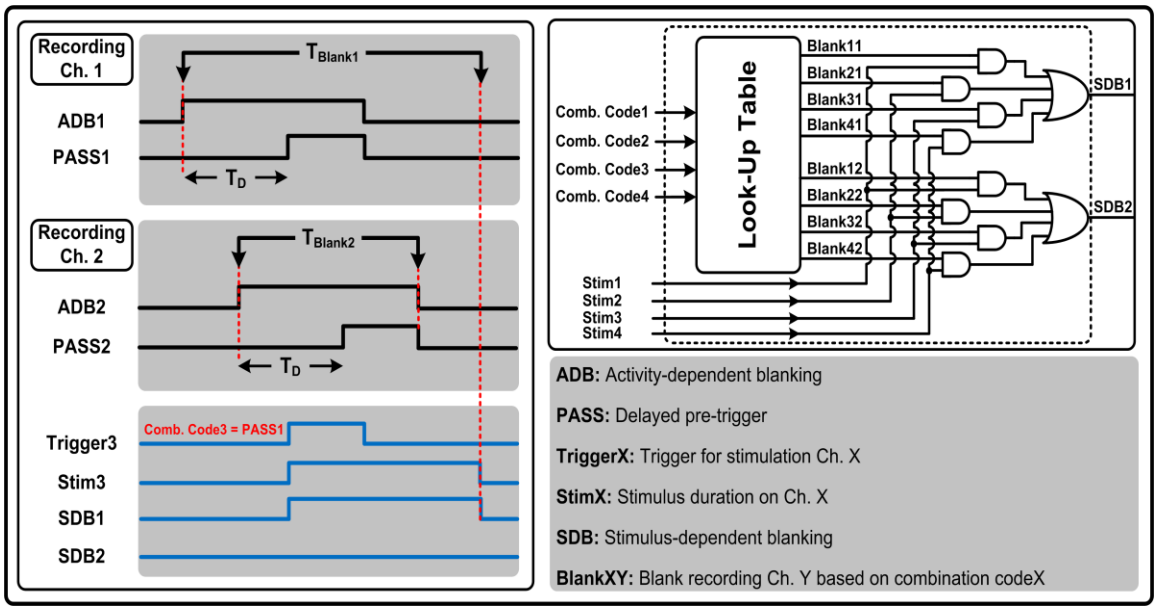

Figure 3.41: Individual blanking mechanism. SDB signals are generated from stim signals and combinations codes. Activation of ADB signals can blank the channels and also results in stimulation (activation of Stim signals). This again results in prolonged blanking by activating SDB signals in a blanking loop.

3.3.2. Blanking Scheme for Sequential Triggering

In a sequential triggering scenario, all stimulating channels (e.g., four in Fig. 3.1) are engaged, which leads to overall stimulus duration of several seconds per trigger, depending on the user-set parameter T_{D_Stim} (≤ ~1 second). Hence, a blanking scheme is devised to disregard the input neural data on all recording channels until the end of stimulus duration.

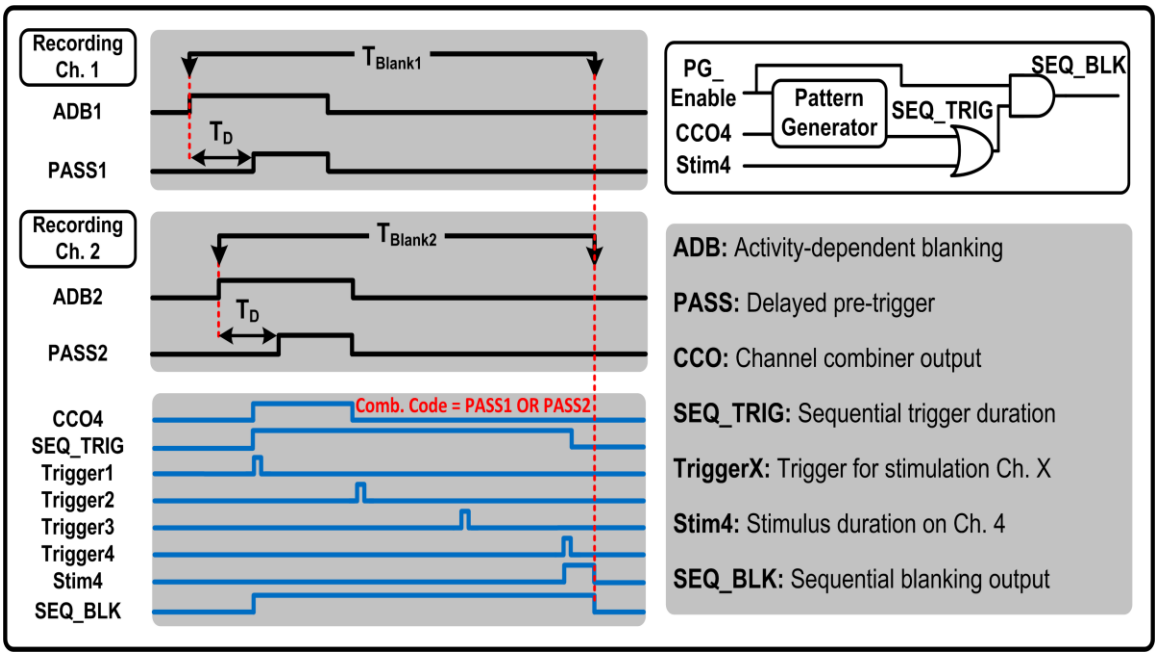

Figure 3.5: Sequential blanking mechanism illustration. Activation of ADB signals can blank the channels and also might result in sequential stimulation which ultimately leads to blanking all the channels for the entire stimulation period. Blanking starts at different time but ends simultaneously for all the recording channels.

As a representative case, Fig. 3.5 illustrates various signals and their relative timings that are involved in blanking for sequential triggering, initiated when trigger-generation criteria are satisfied on at least one input data channel (i.e., *CCO4* is set as the logic OR function of the two *PASS* signals.) The figure also shows how a sequential blanking output signal, *SEQ_BLK*, is generated by the blanking control unit of the decision maker as the OR function of two internal signals (*SEQ_TRIG* from the pattern generator block and *Stim4* from the stimulator controller of the BMBI system) in such a way that *SEQ_BLK* is active throughout the duration of sequential stimulation. Note that the *PG_Enable* signal is always active for sequential triggering, as previously stated in Section III.D.

The *SEQ_BLK* signal is subsequently used to operate a 2:1 multiplexer at the front-end of the neural spike discriminator, as shown in Fig. 3.3. When *SEQ_BLK* is active throughout the duration of sequential stimulation, the input of the neural spike discriminator is held at a constant level to disregard the multiplexed/digitized input neural data. The two internal clock signals (for Ch. 1 and Ch. 2) are also de-activated in the timing & data manager unit to further save power during blanking.

3.4. Implementation and Measurement

The proposed algorithm has been synthesized and mapped to the Cyclone II FPGA, EP2C35F672C6, using Altera's Quartus II design software.

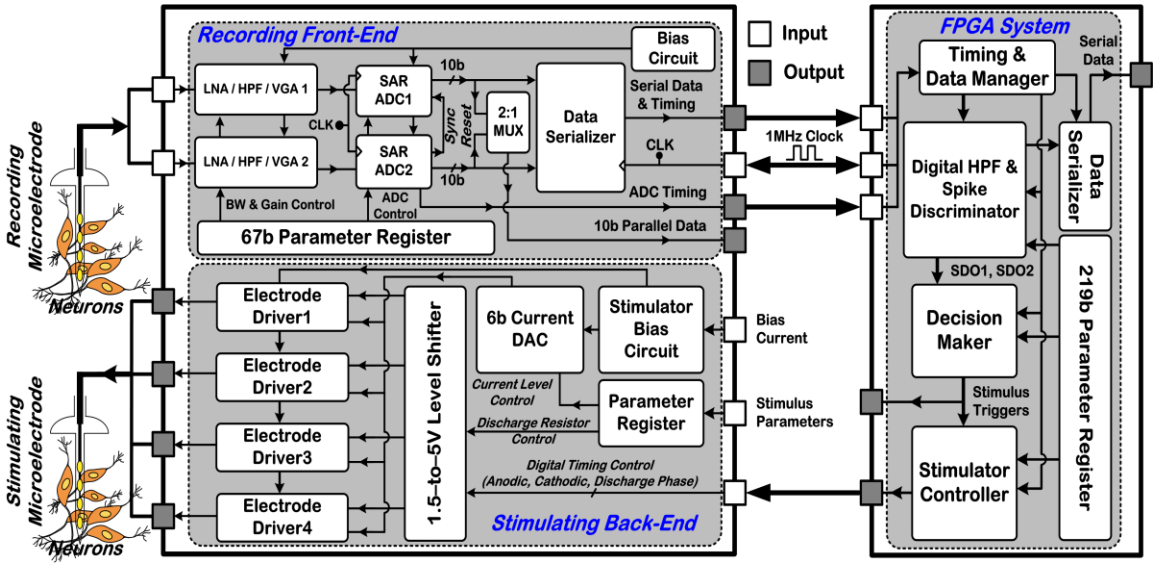

Figure 3.6: System architecture of the interfaced *SCI_Gen1*device and reconfigurable FPGA platform for real-time ISMS trigger generation.

The mapped circuitry consumed 5% (1,661) of the total available logic elements (LEs), 1,172 registers, and a total of 41 I/O pins.

For validating implemented algorithm, FPGA was interfaced with *SCI-Gen1* chip as a brain machine spinal cord interface (BMSI) as shown in Fig. 3.6 [3.2]. With this setup, *in vitro* and *in vivo* experiments have been conducted to verify the functionality of the proposed algorithm.

3.4.1. Benchtop Characterization

Intracortical neural spike activity prerecorded from a laboratory rat's cerebral cortex was fed to the *SCI_Gen1* IC, amplified, filtered, and digitized output was fed to FPGA platform, and trigger generation results under three different scenarios were captured on a home-based computer using a digital data acquisition (DAQ) card (NI 6541, National Instruments). The setup is shown in Fig. 3.7.

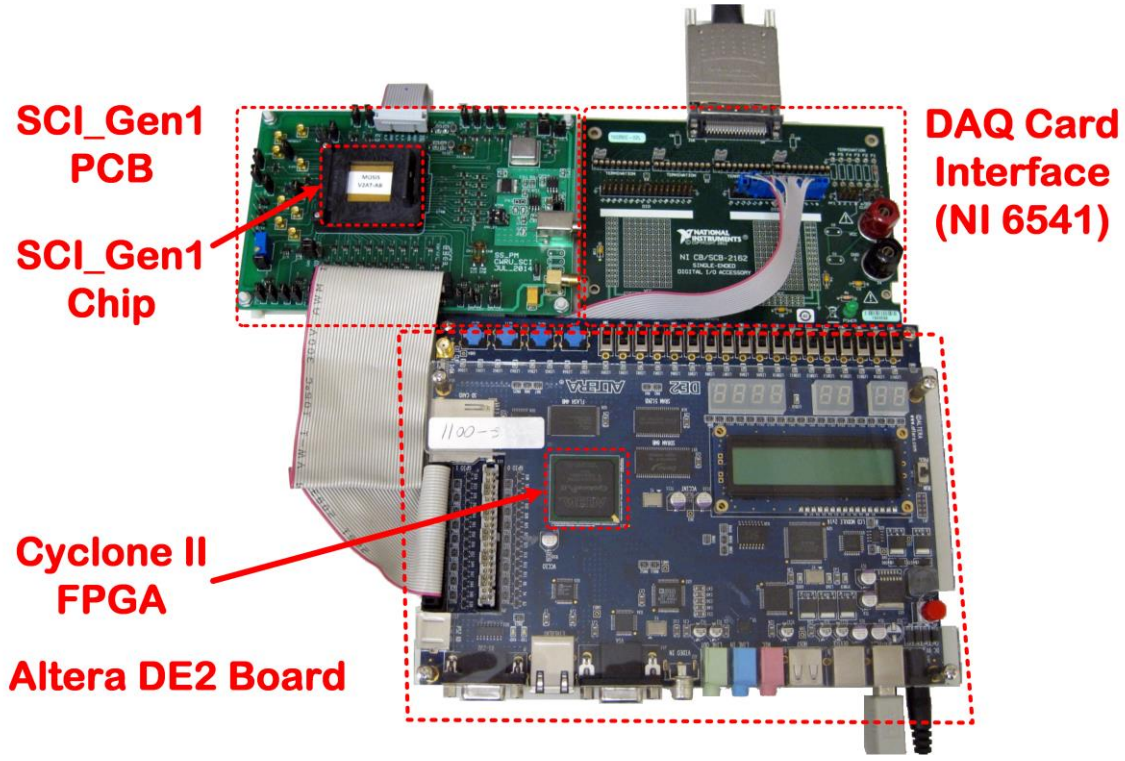

Figure 3.7: The measurement setup; prerecorded data is amplified by the chip and serves as the input for implemented algorithm on FPGA. Generated triggers are fed back to the chip for delivering charge balanced biphasic or monophasic stimulation pulses with passive discharges.

In the first scenario, the FPGA platform was programmed to generate multiple triggers for sequential, multichannel stimulation based on discriminating two neural spikes within a time bin of 0.35 seconds, with a delay of 20ms from spike discrimination to generation of the first trigger. Fig. 3.8 shows the measurement results from the FPGA platform under this scenario. The SDO trace indicates the discrimination of two neural spikes (in <0.15 seconds) upon which a set of four sequential triggers with a user-set inter-channel delay of T_{D_Stim}=200ms were generated after a time delay of 20ms from the discrimination of the second spike.

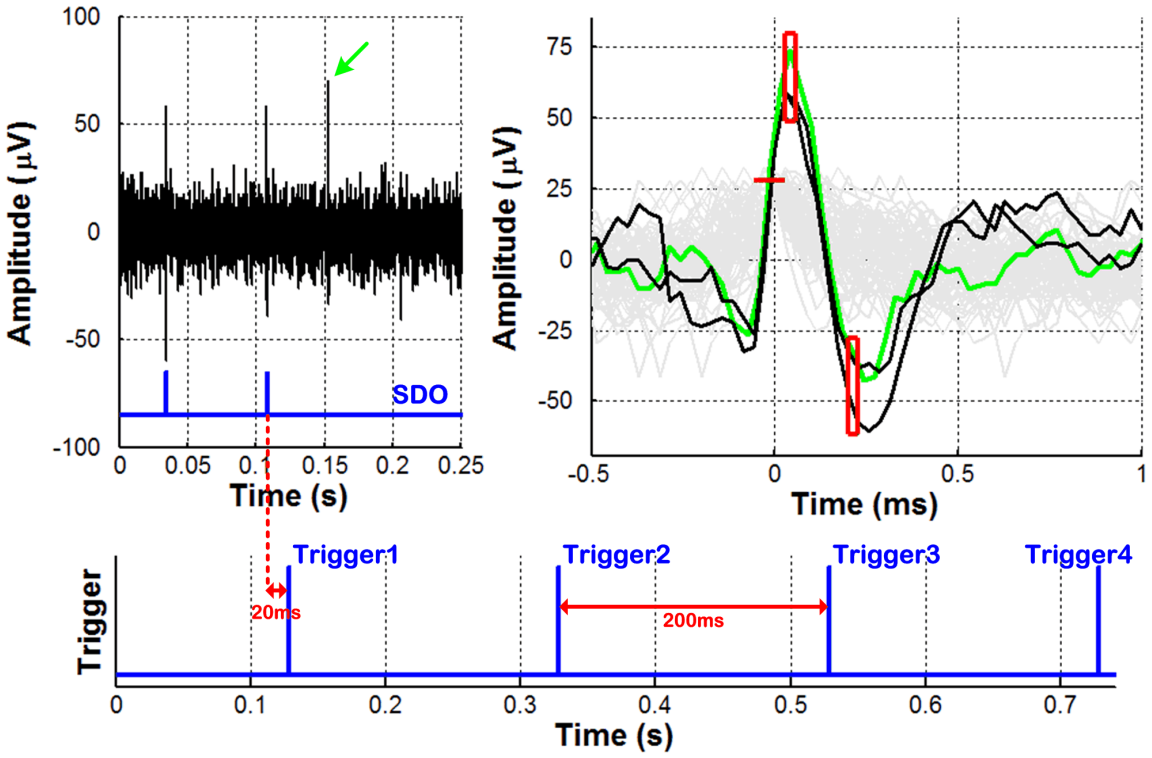

Figure 3.8: FPGA measurement results; Multichannel trigger generation for sequential stimulation based on discrimination of two intracortical neural spikes from a rat's cerebral cortex.

A close-up view of the two discriminated spikes in dark grey is also shown after thresholding and time-amplitude windowing. The spike shown with green arrow is

blanked by SDB mechanism. As shown in green color in the extracted spikes, the blanked spike passes the time amplitude windows.

In the second scenario, FPGA platform was programmed to generate two sequential triggers for multichannel stimulation on channel 1&2 and with a 0.3 second delay, stimulation on channels 3&4 after discriminating 5 neural spikes in 0.4 second.

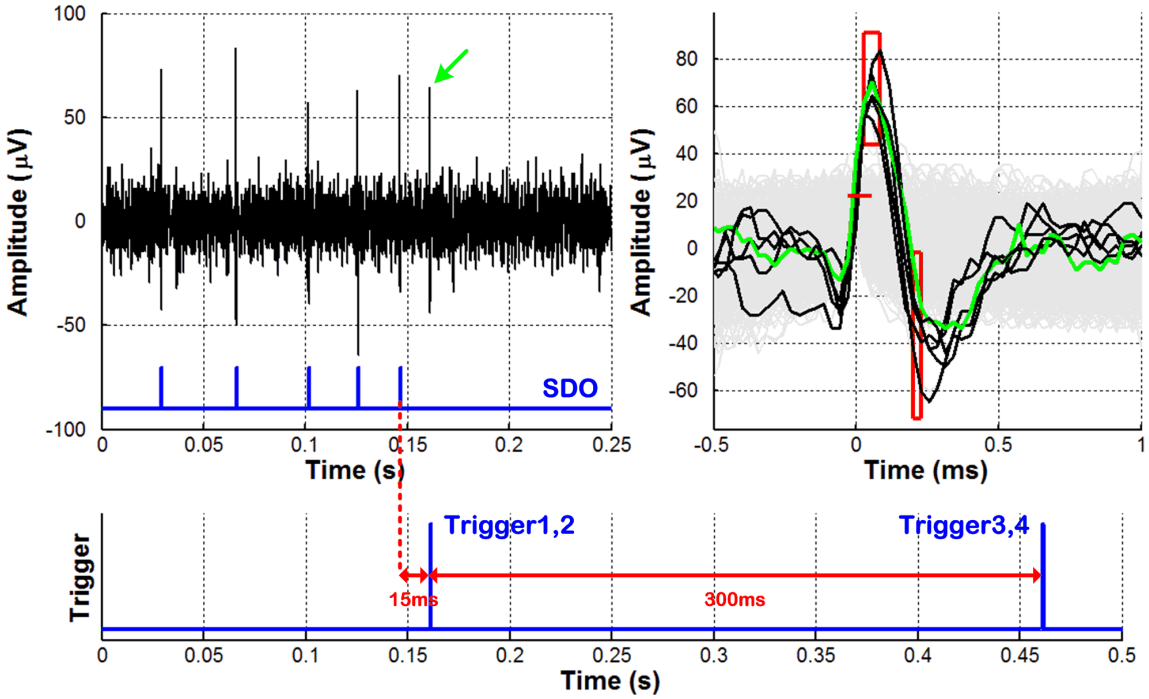

Figure 3.9: FPGA measurement results; Multichannel trigger generation for paired sequential triggering. Green spike occurred during the blanking period, so did not affect any ongoing process.

Fig. 3.9 shows the measurement results from the FPGA platform under this scenario. The SDO traces show discrimination of 5 neural spikes in less than 0.2 second and trigger for first two channels was generated 15ms after the last spike. Fig. 3.9 also shows an expanded view of the five discriminated spikes (in dark grey) that crossed the positive threshold level and subsequently passed through both user-adjustable time-amplitude windows, along with a green trace that shows an acceptable spike by time-

amplitude windows which has occurred in the blanking period of the algorithm. This spike is also marked with a green arrow in the neural activity on top left of Fig. 3.9.

In the last scenario, the FPGA platform was programmed to generate one trigger signal for simultaneous, multichannel stimulation based on discriminating a total of six neural spikes within a time bin of 0.42 seconds, with a time delay of 28ms from spike discrimination to trigger generation. Fig. 3.10 shows the measurement results from the FPGA platform under this scenario. Similar to the previous case, the SDO traces shows six neural spikes were discriminated (in fact, in <0.25 seconds), and one trigger signal was generated with a delay of 28ms after the discrimination of the last spike.

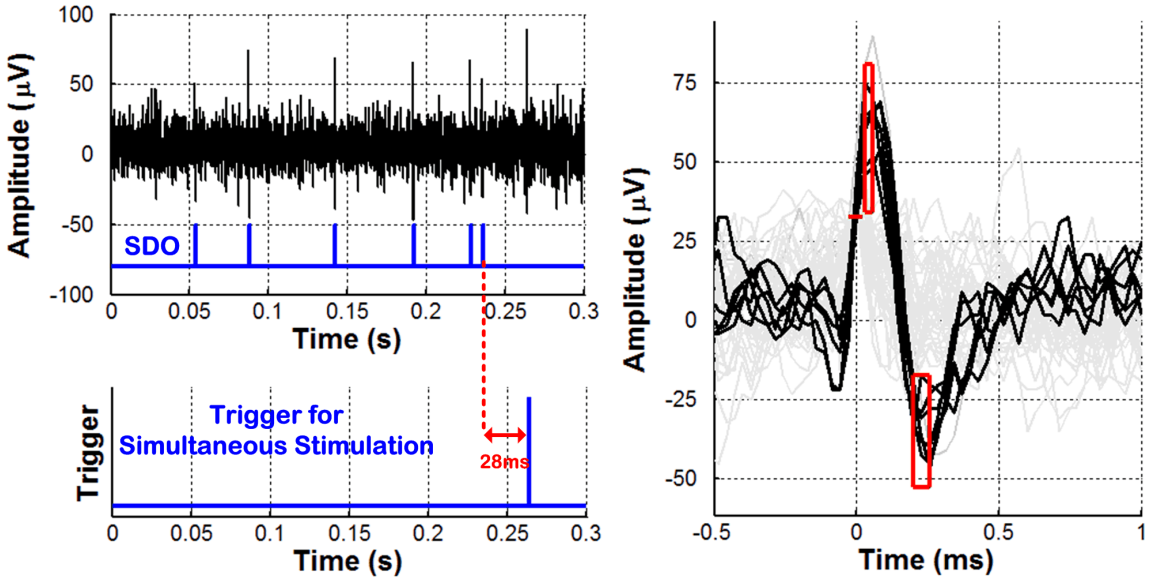

Figure 3.10: FPGA measurement results; multichannel trigger generation for simultaneous stimulation.

Fig. 3.10 also shows an expanded view of the six discriminated spikes (in dark grey) that crossed the positive threshold level and subsequently passed through both user-adjustable time-amplitude windows. The signal waveforms in light grey were rejected by

the FPGA platform for trigger-generation purposes, as they did not satisfy all criteria for discrimination at the same time.

3.4.2. *In Vivo* Experiments

Neurobiological experiments were performed in healthy, anesthetized rats in accordance with guidelines approved by the Institutional Animal Care and Use Committee (IACUC) at the University of Kansas Medical Center. Fig. 3.11 depicts fine-wire electromyography (EMG) signals that were recorded from 3 hind limb muscles while sequential, multichannel ISMS was controlled by intracortical neural spikes and delivered to the lumbar spinal cord through an acutely implanted microelectrode array. Specifically, the FPGA was configured to generate multiple triggers for sequential, multichannel ISMS (inter-channel delay, T_{D_Stim}=100ms) for each discriminated neural spike (i.e., N = 1) with a delay of 20ms from spike discrimination to generation of the first trigger. The corticospinal interface IC was programmed for ISMS with a single monophasic current pulse (anodic, 35μA, 200μs) followed by passive discharge. Throughout the stimulation duration, BMSI operation was blanked to disregard any artifacts generated by the stimulus pulses. ISMS consistently activated the gluteus medius and lateral gastrocnemius muscles but did not activate the vastus lateralis muscle, indicating a specific muscle response at a precise location within the spinal cord. This demonstration of specificity suggests that it may be possible to achieve desirable muscle activation sequences by targeting ISMS to precise locations that can be identified through intraspinal mapping. Fig. 3.11 also shows an expanded view of all spikes in a 3-second window that were successfully discriminated (dark gray) by thresholding and two time-

amplitude windows. Red markers point to the two discriminated neural spikes that triggered ISMS in the rat.

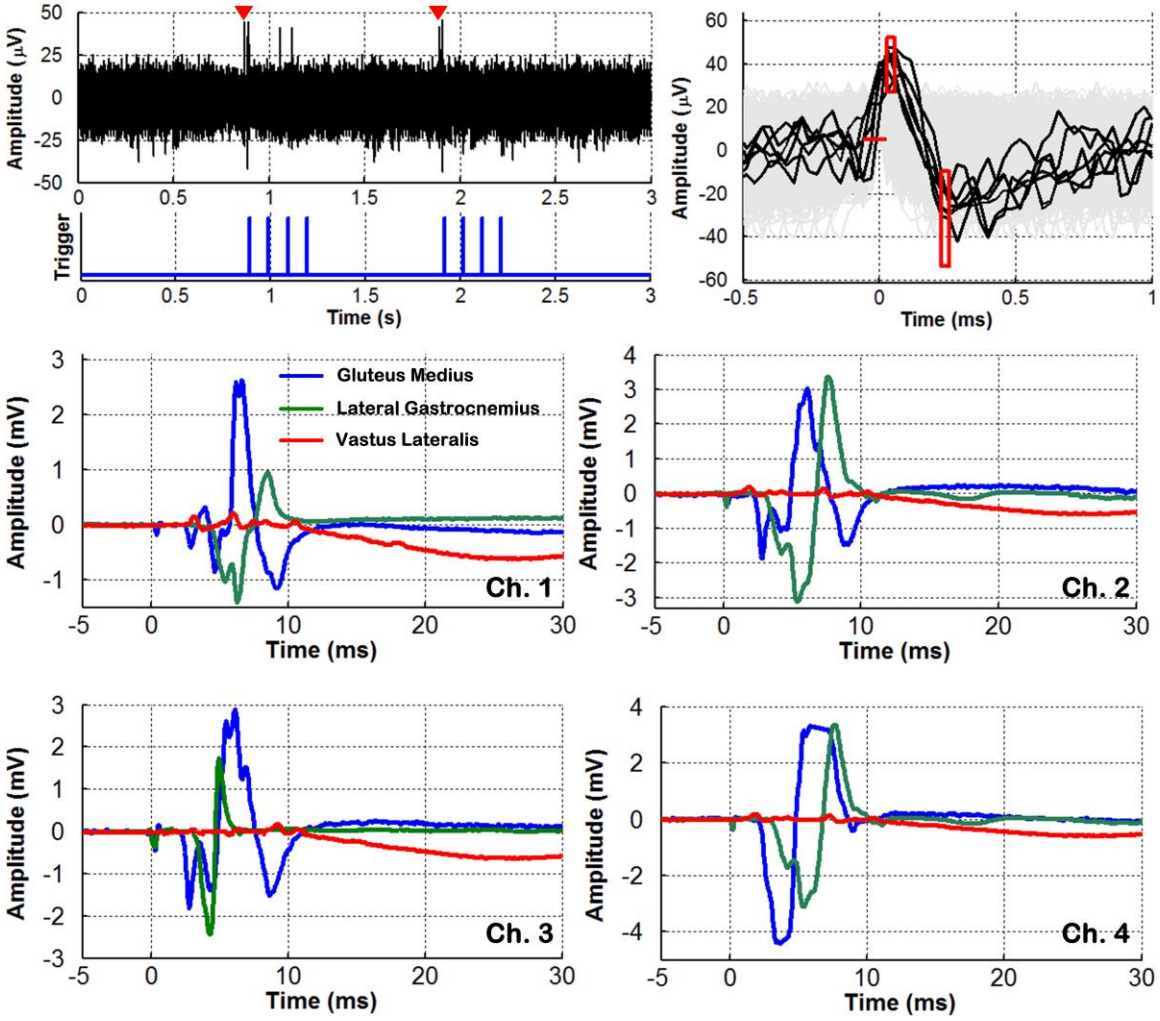

Figure 3.11: Top – Trigger generation for sequential, multichannel ISMS in the rat based on real-time discrimination of intracortical neural spikes from the rat's cerebral cortex. Bottom – Recorded EMG signals from 3 hindlimb muscles of the rat activated via closed-loop, cortically controlled, sequential, multichannel ISMS in the rat.

Fig. 3.12 shows our results from a second experiment involving *simultaneous*, multichannel ISMS in the rat controlled in real time by discriminated neural spikes from the rat's cerebral cortex (N = 1). The spike-to-stimulus delay and stimulus current level were reduced to 10ms and 15μA, respectively.

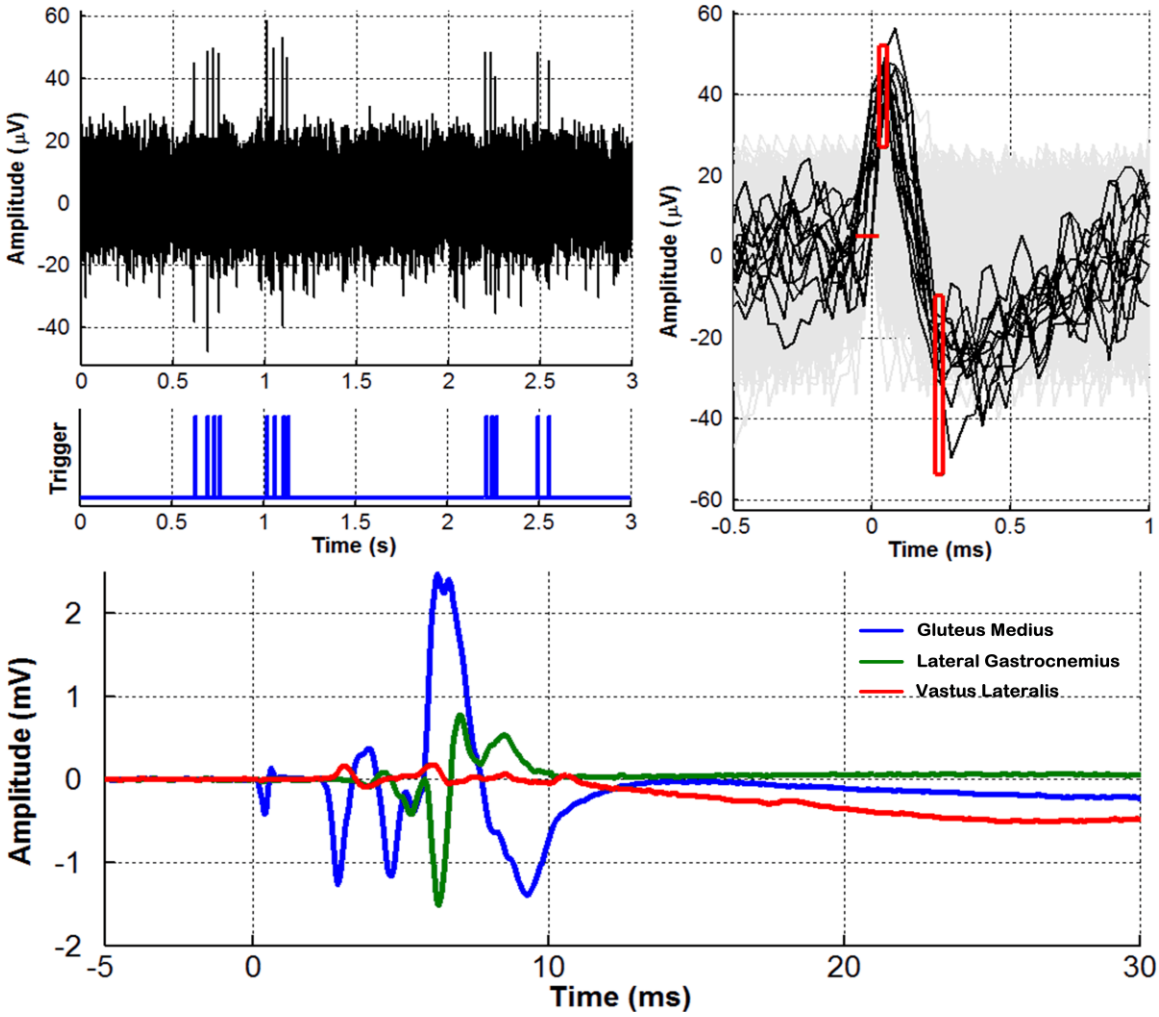

Figure 3.12: Top – Trigger generation for *simultaneous*, multichannel ISMS in the rat based on real-time discrimination of intracortical neural spikes from the rat's cerebral cortex. Bottom – Recorded EMG signals from 3 hind-limb muscles of the rat activated via closed-loop, cortically controlled, simultaneous, multichannel ISMS in the rat.

3.5 References for Chapter 3

[3.1] S. Shahdoost *et al*., "Towards a miniaturized brain-machine-spinal cord interface (BMSI) for restoration of function after spinal cord injury," *2014 36th Annual International Conference of the IEEE Engineering in Medicine and Biology Society*, Chicago, IL, 2014, pp. 486-489.

[3.2] S. Shahdoost and P. Mohseni, "An FPGA platform for generation of stimulus triggering based on intracortical spike activity in brain-machine-body interface (BMBI) applications," *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, Lisbon, 2015, pp. 1766-1769.

[3.3] S. Shahdoost *et al*., "Cortical control of intraspinal microstimulation: Toward a new approach for restoration of function after spinal cord injury,"*2015 37th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*, Milan, 2015, pp. 2159-2162.

[3.4] Shahdoost, S.; Nudo, R.; Mohseni, P., "A brain-machine-spinal cord interface (BMSI) for functional recovery after spinal cord injury," in Student Research Preview Session (SRP), International Solid State Conf., ISSCC, San Francisco, CA, Feb. 2015.

[3.5] S. Shahdoost, R. J. Nudo and P. Mohseni, "Generation of Stimulus Triggering from Intracortical Spike Activity for Brain-Machine-Body-Interfaces (BMBIs)," in *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, vol. 25, no.7, pp. 998-1008, July 2017.

Chapter 4

Miniaturized Brain-Machine-Spinal Cord Interface (BMSI) SoC for Closed-Loop Intraspinal Microstimulation

In previous chapters, we have presented our work on developing a system-on-chip (SoC) for robust recording of intracortical neural activity and intraspinal microstimulation; *SCI_Gen1*. Besides, field-programmable gate array (FPGA) implementation of a digital signal processing (DSP) unit for real-time generation of the stimulus triggering from intracortical neural activity has been thoroughly discussed. In this chapter, we build upon our expertise, knowledge, and device functionality from previous chapters, and present a 3.45 × 3.45mm^2 SoC, *SCI_Gen2*, fabricated in AMS 0.35µm 2P/4M CMOS technology as a miniaturized brain-machine-spinal cord interface (BMSI) for closed-loop control of intraspinal microstimulation. In particular, the SoC uniquely integrates intracortical neural recording as its recording front-end, on-the-fly digital signal processing, and intraspinal microstimulation as its stimulating back-end to investigate the possibility of functional recovery after spinal cord injury (SCI) in rat model of SCI.

The SoC incorporates a 32µW custom-designed DSP unit for real-time processing of intracortical neural data obtained by four recording channels in each module in the *SCI_Gen2* to generate appropriate triggers and requisite control signals for four intraspinal stimulating channels in the back-end.

The *SCI_Gen2* shares the same architecture with *SCI_Gen1* for the recording and stimulating channel in its front-end and back-end with minor modifications in circuit and layout levels. Also the DSP unit shares the same architecture with the implemented DSP on the FPGA in the previous section with system level modification to expand its operation to a four by four recording-stimulating channel system.

The rest of this chapter is organized as follows; section 4.1 presents the system architecture of *SCI_Gen2*, section 4.2 discusses the design and architecture of key building blocks within the SoC, and section 4.3 presents our measured results from benchtop testing and biological experiments with SCI anesthetized rats.

4.1 Integrated Microsystem: System Architecture

Fig. 4.1 shows the suggested architecture for our proposed proof-of-concept BMSI system along with its timing operation, incorporating two identical four-channel modules each compromising four recording channels in the recording front-end, one digital signal processing (DSP) unit, and four stimulation channels in the stimulating back-end [4.1]-[4.2].

Each channel of analog recording front-end, with fully programmable gain and bandwidth, enables the BMSI with robust recording of intracortical neural activity within the frequency range of 100Hz up to 10kHz, and outputs a filtered 10-bit digitized data for

further processing. The DSP unit filters the recorded data in the digital domain using an infinite impulse response high-pass filter (IIR-HPF) and extracts the action potentials (neural spikes) in real-time on each recording channel employing thresholding and two user-adjustable time-amplitude windowing. Afterwards, based on the number of detected spikes on each channel within a programmable duration with a variety of user-adjustable settings, DSP unit generates sequential or individual stimulus triggers from recorded neural activity. Implemented as the last block in the DSP unit, stimulator control block uses generated trigger signals as input, and outputs requisite timing control signals for the stimulating back-end to deliver trains of intraspinal microstimulation (ISMS) with programmable number of pulses and durations in each train. The four-channel stimulating back-end uses generated timing signals and delivers asymmetric biphasic or monophasic current pulses with passive discharge to the stimulation sites. Using a 6-bit current steering DAC, the current amplitudes can be digitally programmed up to ~100μA and ~33.3μA in anodic and cathodic phases, respectively with output impedance of >100MΩ.

As a stand-alone system, two modules in the BMSI also share an integrated clock generator, biasing circuitry, and a radio-frequency frequency-shift-keyed (RF-FSK) transmitter. The clock generator block provides the system clock at a nominal system clock frequency of 1 MHz with a 5-bit programmable frequency. The RF-FSK transmitter operates at 433MHz and can operate in three modes, as shown in Fig. 4.1. In one mode, it transmits the digitized recorded raw data or high-pass filtered data on one channel together with its corresponding spike discriminator output (SDO) signal. In this mode, a 3-bit preamble is scrambled within the data for synchronization purposes between the transmitter and an external receiver. In other two modes, it either transmits

the spike discrimination or the trigger events on all eight channels along with a 6-bit preamble in each data stream. Besides, all the programming and control bits are provided via an integrated 874-bit latched shift register for the proper operation of different building blocks of the BMSI.

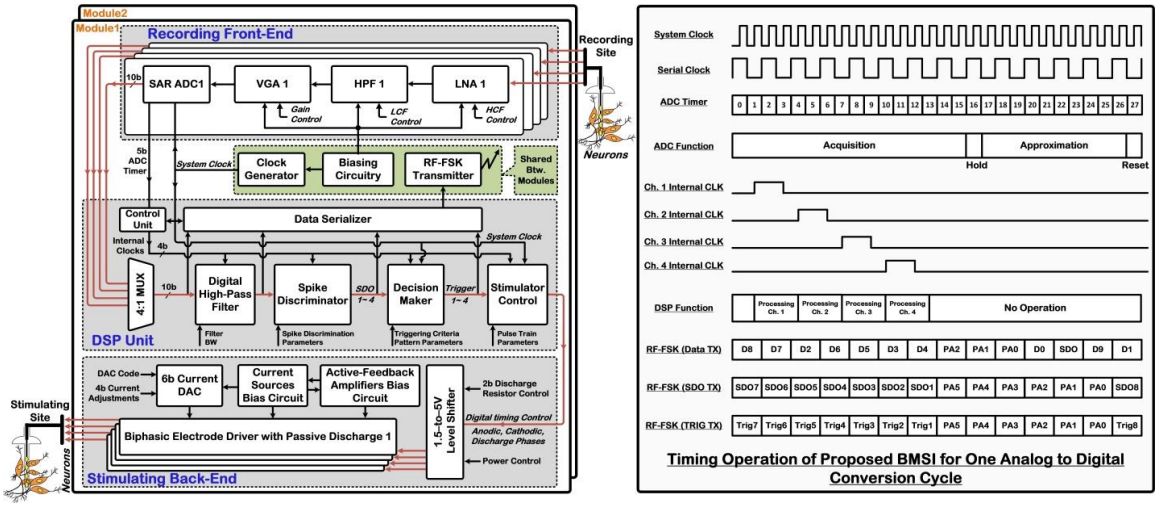

Figure 4.1: Proposed system architecture and timing diagrams of the proposed *SCI_Gen2* BMSI system. There are two identical four-channel modules in the BMSI that share a clock generator, biasing circuit, and a FSK-TX.

Fig. 4.1 also depicts the timing operation of the analog to digital converter (ADC) and the DSP unit for one cycle of ADC conversion. Each ADC conversion takes 28 clock cycles which with nominal system clock frequency of 1MHz, results in sampling frequency of 35.7 KS/s. In addition to the 1MHz system clock provided by clock generator, DSP unit also generates one internal clock from the ADC timer information for each channel for internal operations. Each internal clock takes two clock cycles, and DSP operation for processing data of each channel takes only three clock cycles. Moreover, a data serializer in the DSP unit extracts a 500kHz serial clock from the system clock to

send out the raw/filtered data, SDO signals, and trigger signals to the RF-FSK transmitter and/or external pads.

4.2 Integrated Microsystem: Circuit Architecture

4.2.1 Analog Recording Front-End

Each module of the BMSI has four identical recording channels in the recording front-end. As shown in Fig. 4.1, each recording channel consists of a low-noise amplifier (LNA), an analog G_m-C high-pass filter (HPF), a secondary variable-gain amplifier (VGA), and a 10b successive approximation register analog to digital converter (SAR-ADC). In our design, LNA provides 32dB fixed gain via capacitive feedback and stabilizes the dc-baseline of the signal by using a MOS-bipolar pseudo resistor in parallel with the feedback capacitor.

By digitally tuning the current in HPF and LNA, low cutoff frequency (LCF) and high cutoff frequency (HCF) of the recording front-end can be set within the range of 1.1–525 Hz and 5.1–12.2 kHz, respectively. The VGA can provide additional gain of 20.2dB up to 33.7dB via its 2-bit programmable resistive feedback.

Sampling frequency of 35.7 kS/sec, resulted from 28 clock cycles for a complete analog to digital conversion from a 1MHz clock signal, makes the implemented SAR-ADC suitable for recording intracortical spike activity signals with frequency components of up to 10 kHz. To relax current driving capability of the VGA, for low-power operation, acquisition period is extended up to 16 clock cycles. The ADC digitizes the amplified/filtered neural data with a signal-to-noise and distortion ratio (SNDR) of 56.5 dB (i.e., ENOB of 9.1b) at a maximum sampling frequency of 63kSa/s [4.3].

4.2.2 DSP Unit

Overall architecture of the proposed DSP unit is shown in Fig. 4.1 which incorporates a control unit, digital high-pass filter (HPF), neural spike discriminator, decision maker, data serializer, and stimulator control as its building blocks.

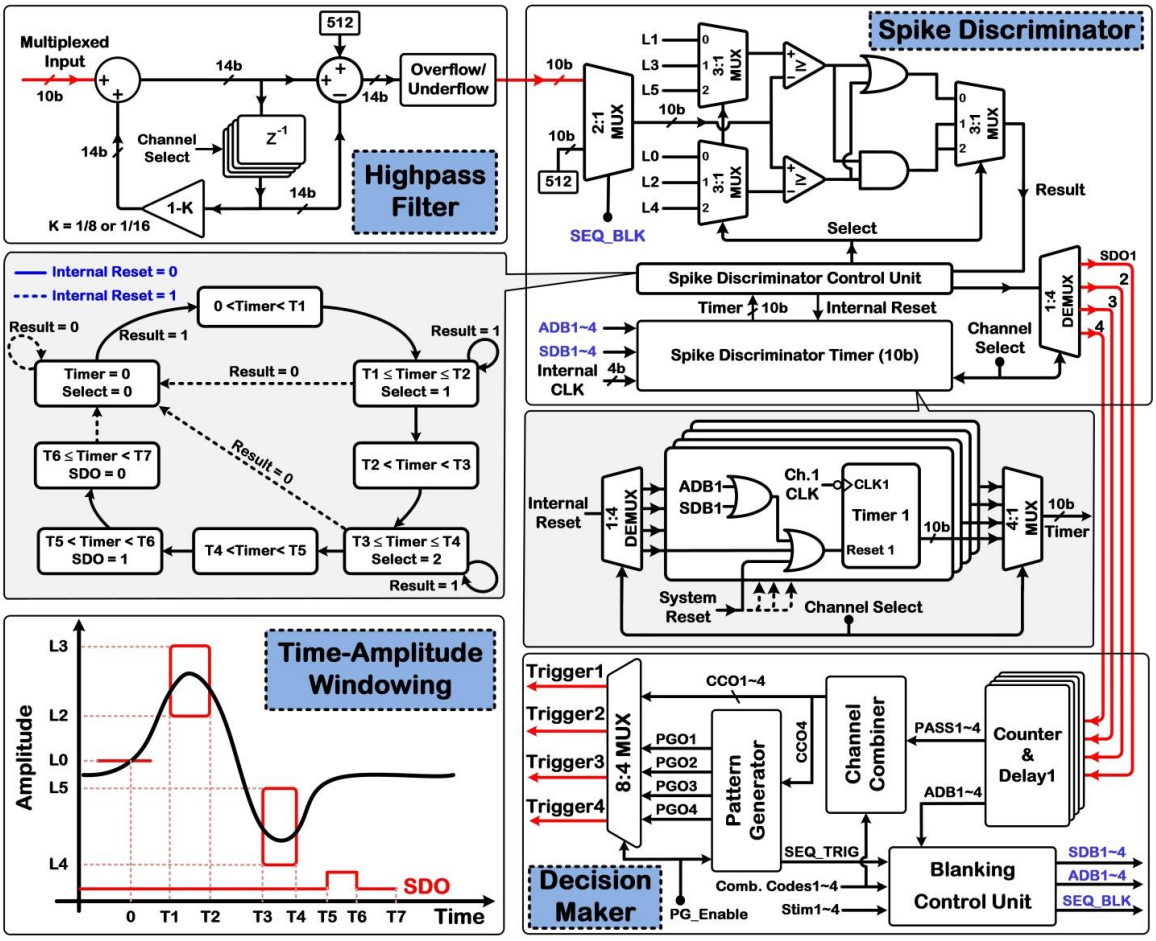

Figure 4.2: Detailed architecture of HPF, spike discriminator, and decision maker of the proposed DSP unit of the BMSI system along with finite state machine (FSM) representation of the spike discriminator control unit and timer structures.

The control unit receives ADC timer information to generate internal clocks for each channel with duration of two clock cycles for internal operation of sub-blocks in the

DSP unit. The data serializer is in charge of sending serialized raw and filtered data, SDO signals, and trigger signals to the RF-transmitter and/or external pads.

As shown in Fig. 4.2, DSP unit shares the same building blocks and ground-rule architecture with the FPGA implementation of DSP unit discussed in Chapter 3, by expanding its operation for on-the-fly processing of four input channels.

4.2.3 Stimulating Back-End

The proposed architecture for the BMSI system consists of a stimulating back-end which incorporates four identical electrode drivers in each module to deliver ISMS trains of monophasic or asymmetric biphasic current pulses followed by passive discharge. Electrode drivers, operating from 5V supply, share a 6b current steering DAC (operating from 1.5V) which has a 4b current adjustment mechanism for fine-tuning the output current. Each electrode driver can deliver anodic pulses (from integrated pMOS current source) of up to ~100μA and cathodic pulses (from integrated nMOS current source) of up to ~33.3 μA to the stimulation sites. Moreover, each electrode driver employs g_m-boosted active feedback circuit to increase their output impedances (>100MΩ.) Each ISMS pulse, monophasic or biphasic, is followed by passive discharge to drain the accumulated charge on the stimulation site using a 2-bit programmable resistor (4.6 to 32 KΩ). During passive discharge, the current DAC and all biasing circuitry are powered down to reduce the static power consumption.

All the timing signals from stimulator control block in the DSP unit, as well as control bits for power management and discharge resistors are shifted from 1.5V to 5V for proper operation by a voltage level-shifter.

4.2.4 Clock Generator

Fig. 4.3 shows the transistor-level schematic of the clock generator for generating a 1-MHz system clock in the implemented BMSI system. Similar circuit was first reported in [4.3]. The clock generator includes a start-up circuit, bias circuit, oscillator core, comparator, and an output buffer. The clock frequency can be adjusted in the range of 420 kHz and 2.5 MHz via a 5b resistor, while the oscillator capacitance is fixed.

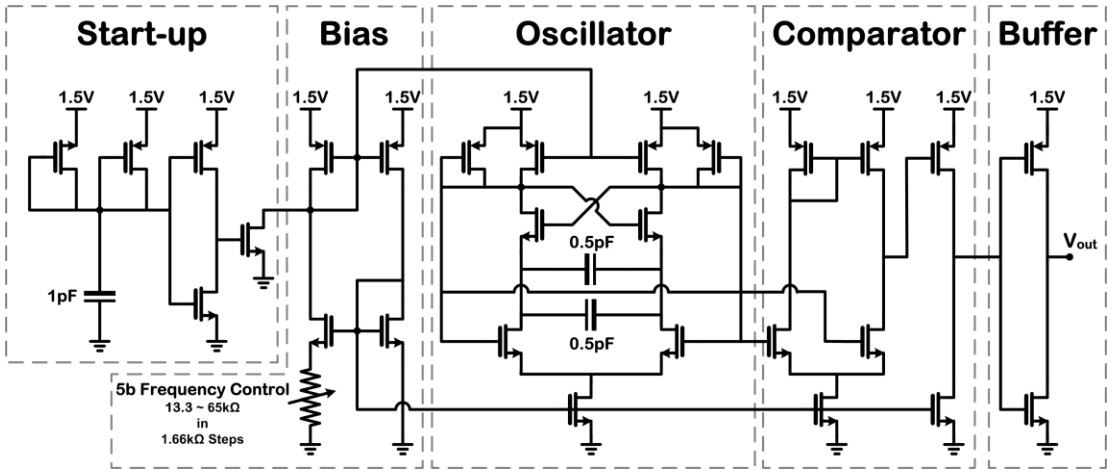

Figure 4.3: Circuit schematic of the clock generator with nominal frequency at 1 MHz [4.3].

The comparator circuit provides rail-to-rail output swing while output buffer guarantees enough driving capability for the system clock tree.

4.2.5 RF-FSK Transmitter

A cross-coupled voltage-controlled oscillator (VCO) with similar architecture to that in [4.3] has been used for RF-FSK transmitter as shown in Fig. 4.4.

An off-chip inductor and capacitor in conjunction with capacitors contributed by wire bonding, packaging, and PCB provides a stable operation frequency near 433 MHz.

The variable capacitor are implemented using NMOS transistors while oscillation frequency (F_{OSC}) and frequency bandwidth (ΔF) can be set via two 2b control signals. Specifically, ΔF can be varied in the range of 0 to 3 MHz in steps of 1 MHz.

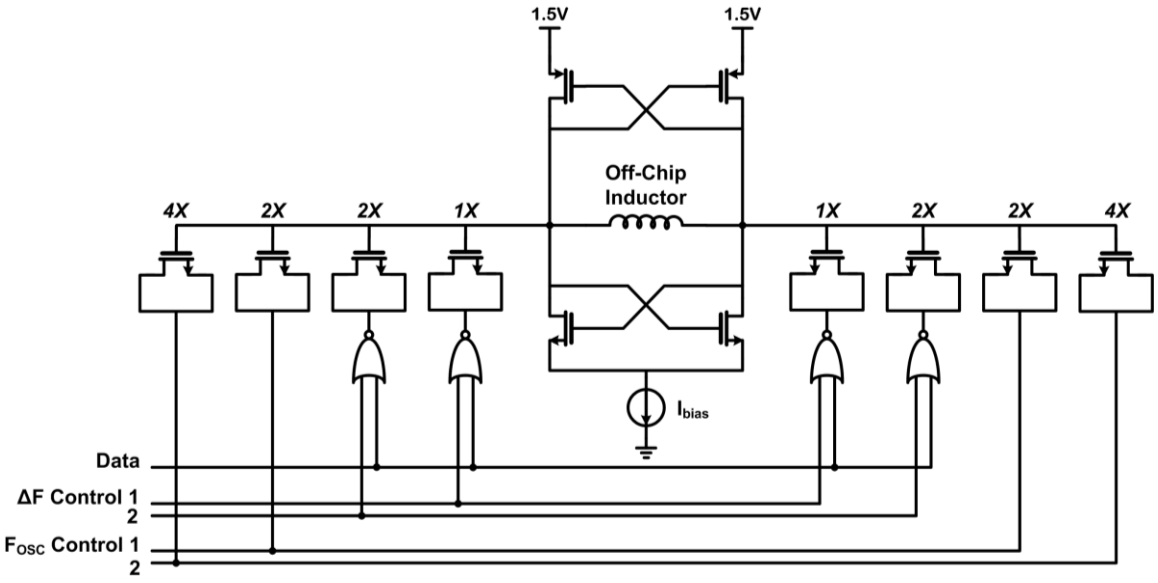

Figure 4.4: Circuit level schematic of the RF-FSK transmitter [4.3].

4.3 Electrical Measurements and Performance Characteristics

A prototype proof of concept IC was fabricated in AMS 0.35µm 2P/4M CMOS technology, measuring ~3.46mm × 3.46 mm including the bonding pads, as shown in Fig. 4.5. Electrical performance of individual circuit blocks was characterized in benchtop measurements, and the BMSI functionality was verified *in vivo* biological experiments with SCI anesthetized laboratory rats.

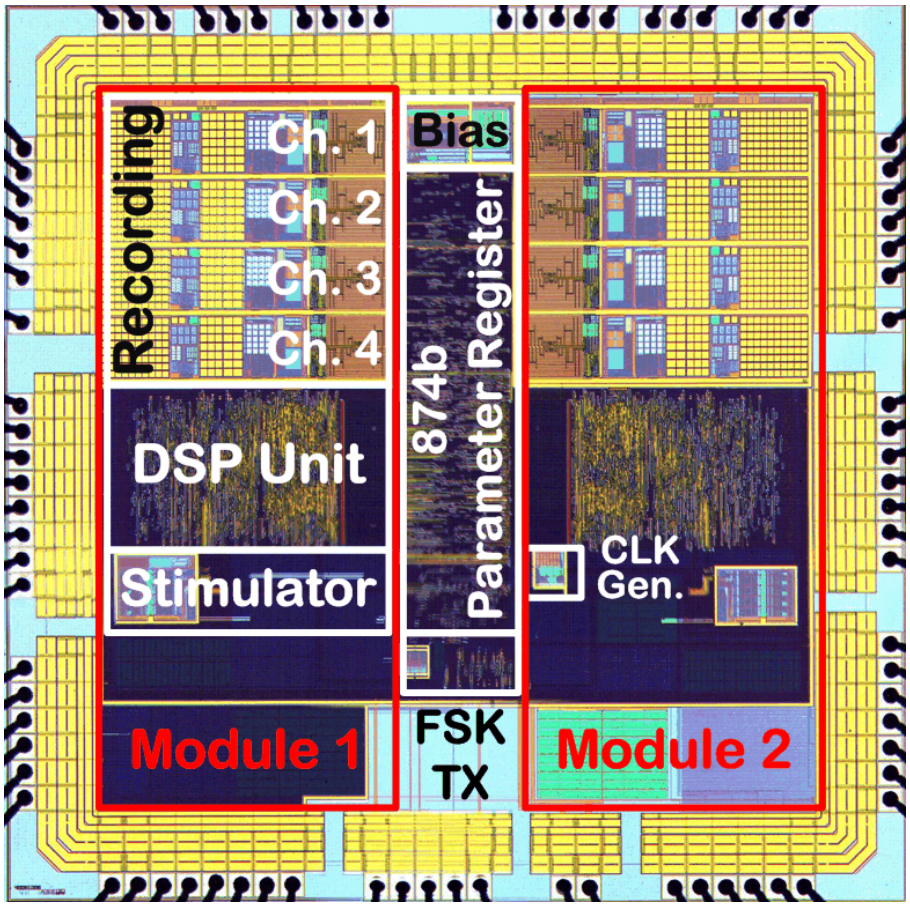

Figure 4.5: Die microphotograph of the *SCI_Gen2* BMSI in 2P/4M AMS 0.35um CMOS.

Plots of measured electrical performance for neural recording front-end are presented in Fig. 4.6. The measured frequency responses for one neural recording channel with three different BW settings are shown in top plot of Fig. 4.6 (a) while the nominal ac gain was set to 60dB. The LCF could vary from 1.1 to 525Hz and the HCF was programmable from 5.1 to 12.2kHz. Besides, each channel has programmable mid-band ac gains of 52.2 to 65.7 dB when the HPF is bypassed.

Fig. 4.6(b) shows the input referred noise voltage of the neural recording front-end for different BW settings. For the maximum BW setting of 1.1Hz to 12.2 kHz, 1/f noise has a significant presence because the HPF was bypassed. With the maximum BW setting,

the total input referred noise voltage in the BW of 0.5Hz to 50 KHz was measured to be 3.15μV_{rms} resulting to a noise efficiency factor (NEF) of 2.69 for the LNA. Besides the flicker noise corner frequency is <100Hz in all bandwidth settings which shows the efficacy of the implemented HPF.

Fig. 4.6 (c) depicts measured signal to noise and distortion ratio (SNDR) for the entire neural recording with respect to input amplitude for four available gain settings at the output of SAR-ADC. Lower gain provides higher dynamic range, while higher gains can result in higher SNDR.

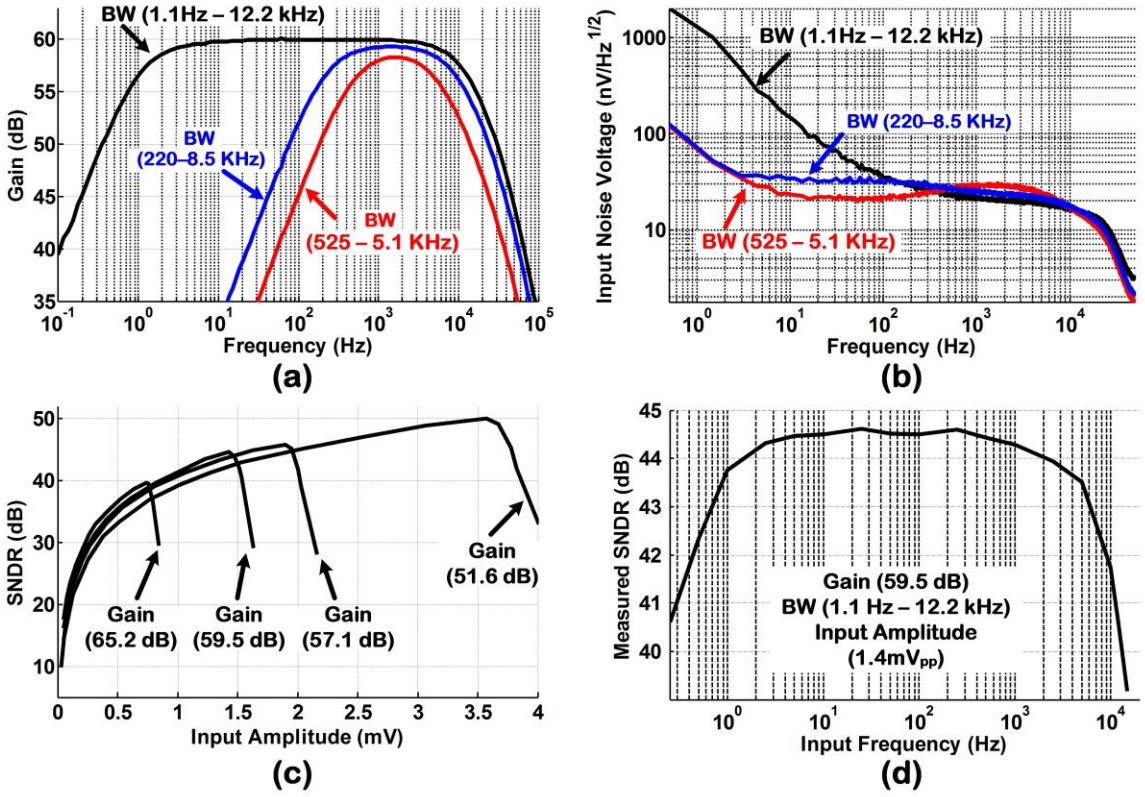

Figure 4.6: Front-end electrical measurements a) Frequency response b) Input referred noise voltage c) SNDR vs. input amplitude d) SNDR vs. input frequency.

Measured SNDR with respect to input frequency is shown in Fig. 4.6 (d) for the maximum BW and gain setting of 59.5 dB with input amplitude of 1.4 mV_{pp}. The

recording front-end can provide >41.8dB SNDR within the frequency range of 100Hz–10kHz of extracellular neural spikes.

Measured electrical performance for stimulating back-end is presented in Fig. 4.7. The top plots in this figure, depicts the measured DNL and INL for the 6b current steering DAC. For the anodic phase DNL and INL were measured to be < ±0.57 LSB and < ±0.56 LSB and for the cathodic phase were < ±0.47 LSB and < ±0.54 LSB, respectively.

Measured stimulator output current versus its output voltage is shown in Fig. 4.7(c) for four input DAC codes (Codes: 63, 32, 16, 8) for both anodic and cathodic phases. The output voltage with the maximum current setting in anodic and cathodic phases could get up to 4.7V and down to 135mV from a 5V power supply while still delivering set constant current.

Fig. 4.7(d) depicts measured asymmetric biphasic stimulus current waveform delivered by the stimulating back-end of the BMSI to saline via microelectrode. Passive discharge is performed in this case using an on chip 32 kΩ resistor. All the timing parameters (T_{Anodic}, $T_{Interchannel\_Delay}$, $T_{Cathodic}$, $T_{Discharge}$) are programmable in the chip via stimulator control unit. For T_{ID}=$T_{Cathodic}$=0, BMSI delivers anodic monophasic current pulse to the stimulation site with passive discharge.

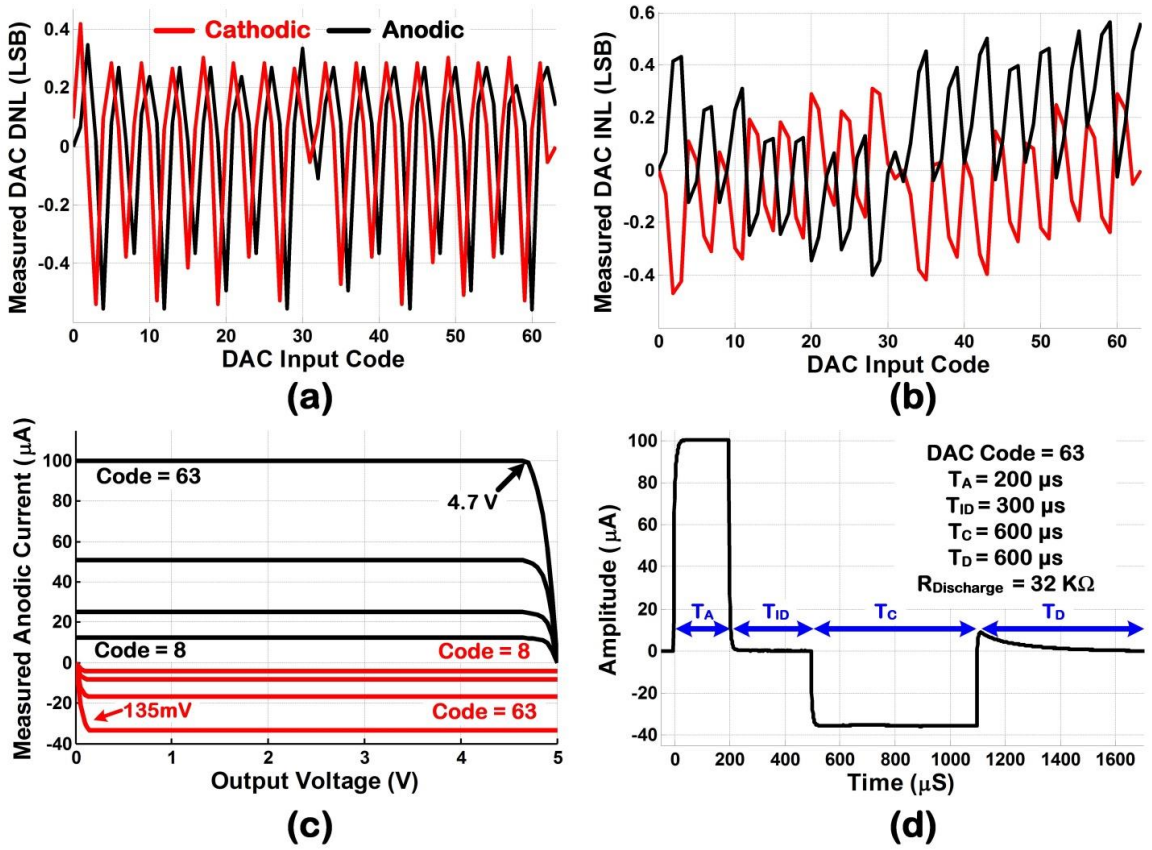

Figure 4.7: Stimulating back-end electrical characteristics; a) DAC DNL b) DAC INL c) output current versus output voltage for codes 63, 32, 16, and 8 d) asymmetric biphasic current pulse with the maximum amplitudes.

A receiver operating characteristics (ROC) graph is a well-known technique for visualizing and organizing detectors based on their performance. A window of 1-second data have been synthesized using three different templates of neural spikes with Poisson distribution [4.4] at rate of ~100Hz. Then, the level of White Gaussian noise in the data is adjusted for three different levels of signal to noise ratio (SNR) by defining the SNR as the ratio between the mean of all peak-to-peak values of spikes and six times the standard deviation of the noise [4.5].

True positive rate is defined as the ratio of detected true positives by the total number of available spikes in the signal and false positive rate as the ratio of detected

false positives by the total number of detected spikes by the algorithm. ROC curves are plotted by sweeping the height of time-amplitude windows and calculating true positive rate and false positive rate for each level of SNR as shown in Fig. 4.8.

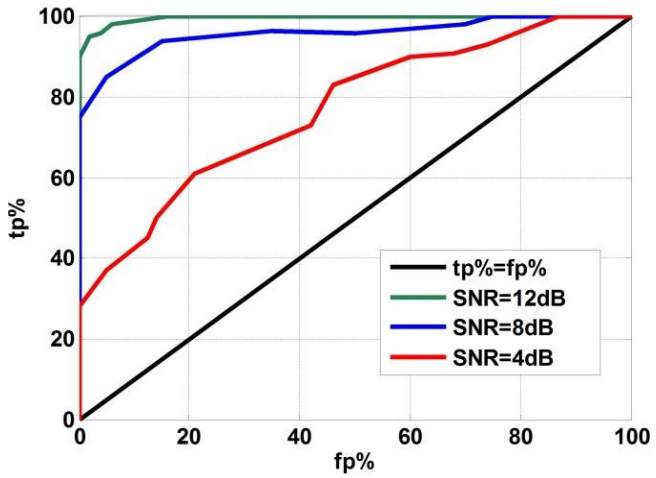

Figure 4.8: ROC curves for the implemented spike discriminator at three different levels of SNR.

Fig. 4.9 shows the breakdown of the silicon area and power consumption for the entire SoC including both modules. The SoC core area, excluding I/O pads, was $2.78\times2.78mm^2$, of which 20% was occupied by the DSP unit, which was implemented using Verilog HDL. As shown in a separate bar chart, 38.5% of the DSP area was occupied by the decision maker excluding the blanking control unit that occupied another1%.

The power pie-chart is generated assuming biphasic stimulation at a rate of 30 Hz (anodic: 100 µA, 200 µs; cathodic: 33.3 µA, 600 µs) and recording bandwidth of 525 Hz to 5.1 kHz. Excluding the FSK transmitter, the total power consumption is measured to be 359 µW for two modules with the analog recording front-end being the most power-hungry circuit block.

In order to breakdown the power consumption of the DSP unit, it was simulated in the Cadence™ environment using the *NCSim* tool using prerecorded neural data obtained in an *in vivo* experiment. The switching activity of the DSP unit was then fed into the Encounter Digital Implementation (EDI) tool to calculate the power consumption of each building block. The overall power consumption of the system was estimated by the EDI tool to be ~34.5µW from a power supply of 1.8V using the typical corner model. This was in good agreement with the measured power of ~32µW from a 1.5 V power supply. Based on the power analysis obtained by the EDI tool, 49% of the DSP power was dissipated in the clock network of the individual building blocks. The leakage power was estimated to be 71nW, and the stimulator control consumed 42% of the overall power of DSP unit.

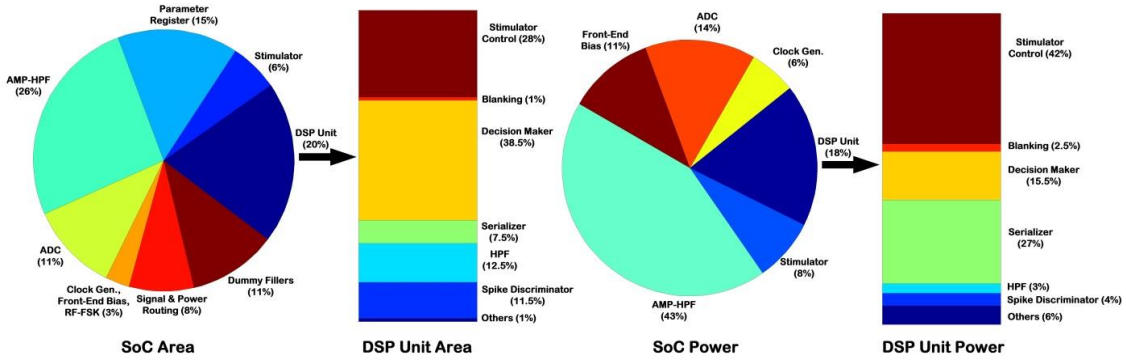

Fig. 4.9: Breakdown of silicon area (excluding I/O pads) and power consumption (excluding FSK-TX) for the BMSI and its DSP unit.

Table 4.1 provides a summary of the specifications and measured performance of *SCI_Gen2* device as a stand-alone BMSI.

Table 4.1: Summary of SCI_Gen2 Specifications and Measured Performance

<table>
<tr><th colspan="2">RECORDING FRONT-END</th><th colspan="3">STIMULATING BACK-END</th></tr>
<tr><td>AC Gain @ 1 kHz</td><td>52.2, 57.5, 60, 65.7 dB</td><td></td><td>Anodic</td><td>Cathodic</td></tr>
<tr><td>Low Cutoff Freq.</td><td>1.1 ~ 525 Hz</td><td rowspan="2">Stimulus Waveform</td><td colspan="2" rowspan="2">Asymmetric Biphasic & Monophasic w/ Passive Discharge</td></tr>
<tr><td>High Cutoff Freq.</td><td>5.1 ~ 12.2 kHz</td></tr>
<tr><td rowspan="2">Total RMS Input Noise Voltage</td><td rowspan="2">3.15 µV (BW of 12 kHz)
3.42 µV (BW of 5.1 kHz)</td><td rowspan="2">Output Current</td><td rowspan="2">0 ~ 100 µA</td><td rowspan="2">0 ~ 33.3 µA</td></tr>
<tr><td rowspan="2">NEF</td><td rowspan="2">2.69 (BW of 12 kHz)
2.9 (BW of 5.1 kHz)</td></tr>
<tr><td rowspan="2">Output Impedance</td><td colspan="2" rowspan="2">> 100 MΩ</td></tr>
<tr><td>Crosstalk</td><td><-69dB</td></tr>
<tr><td>CMRR @ 1 kHz</td><td>>56 dB</td><td rowspan="2">DAC Resolution</td><td colspan="2" rowspan="2">6b</td></tr>
<tr><td>PSRR @ 1 kHz</td><td>>63.4 dB</td></tr>
<tr><td>Max. Sampling Freq.</td><td>63 kS/s</td><td rowspan="3">Voltage Compliance
Monophasic
Biphasic**</td><td rowspan="3">4.7 (of 5 V)
3.2 (of 3.5 V)</td><td rowspan="3">N/A
1.35 (of 1.5 V)</td></tr>
<tr><td>INL/DNL</td><td>< ±0.83 LSB</td></tr>
<tr><td>ENOB</td><td>9.2b (f_{in} = 1 kHz, f_S = 35.7 kS/s)
9.1b (f_{in} = 1 kHz, f_S = 63 kS/s)</td></tr>
<tr><td rowspan="4">Power Consumption
Amp-HPF
SAR ADC</td><td rowspan="4">26.9 µW (BW of 12 kHz)
19.9 µW (BW of 5.1 kHz)
5.9 µW (f_{CLK} = 1 MHz)</td><td>DAC INL</td><td>< ±0.57 LSB</td><td>< ±0.47 LSB</td></tr>
<tr><td>DAC DNL</td><td>< ±0.56 LSB</td><td>< ±0.54 LSB</td></tr>
<tr><td>Supply Sensitivity</td><td>-69 nA/V</td><td>-10 nA/V</td></tr>
<tr><td>Power Consumption</td><td colspan="2">29 µW with max currents (Biphasic @ 30Hz Anod. 200µs – Cath. 600 µs)</td></tr>
<tr><th colspan="5">Digital Signal Processing Unit</th></tr>
<tr><td>HPF Cutoff Freq.</td><td>366 / 756 Hz (f_{CLK} = 1 MHz)</td><td>ISMS Patterns</td><td colspan="2">Sequential (3 modes) - Individual</td></tr>
<tr><td>Max number of spikes (N)</td><td>15</td><td>ISMS Pulse Freq.</td><td colspan="2">> 122 Hz</td></tr>
<tr><td>Bin Duration (T_{Bin})</td><td>~ 0.5 s</td><td>Max number of ISMS pulses/train</td><td colspan="2">31</td></tr>
<tr><td>Spike to stimulus Delay (T_D)</td><td>28.6ms</td><td>Inter-Channel Delay (T_{D_Stim})</td><td colspan="2">~ 1 s</td></tr>
<tr><td>Power Consumption</td><td>32 µW (f_{CLK} = 1 MHz)</td><td>Blanking Schemes</td><td colspan="2">Sequential - Individual</td></tr>
<tr><th colspan="2">Clock Generator</th><th colspan="3">RF Transmitter</th></tr>
<tr><td rowspan="2">Output Frequency</td><td rowspan="2">420 kHz ~ 2.5 MHz</td><td>Comm. Scheme</td><td colspan="2">FSK @ 433 MHz</td></tr>
<tr><td rowspan="2">Received power @ 1m distance</td><td colspan="2" rowspan="2">-55 dBm (18-cm monopole TX and RX Antenna)</td></tr>
<tr><td>Supply Sensitivity</td><td>-60 kHz/V</td></tr>
<tr><td>Power Consumption</td><td>21 µW (f_{CLK} = 1 MHz)</td><td>Power Consumption</td><td colspan="2">200 µW</td></tr>
</table>

4.4 *In Vivo* Experiments

To verify the functionality of the proposed BMSI system, neurobiological experiments were performed in SCI, anesthetized rats in accordance with guidelines approved by the Institutional Animal Care and Use Committee (IACUC) at the University of Kansas Medical Center.

In all the experiments, the BMSI was recording four channel neural activities from the barrel cortex of the rat and delivering monophasic ISMS pulses with passive discharge to the spinal cord below the injury level. Besides, three hind-limb muscles of the rat (namely Biceps Femoris, Vastus Lateralis, and Tibialis Anterior) were implemented with fine-wire electromyography (EMG) electrodes, to record the evoked EMG activity as a result of ISMS by BMSI.

4.4.1 Individual ISMS

Fig. 4.10 depicts EMG signals resulted from closed-loop control of ISMS on stimulating Ch. 4 by the BMSI in an individual triggering scenario. In this case BMSI was programmed to deliver a monophasic current pulse with passive discharge (anodic, 15µA, 200µs) to the rat's spinal cord after successful discrimination of two neural spikes (N=2) on recording Ch.1 within a time bin duration of ~ 0.5s and spikes to stimulus delay of 25ms. In the left plots, recorded neural activity on Ch. 1 of BMSI along with generated SDO1 and Trigger4 signals during the experiment are depicted. In the top right plot, neural spikes (black) after offline thresholding and time-amplitude windowing (red solid boxes) are shown. The light grey signals passed the threshold level but did not pass through the time-amplitude windows and were rejected. Moreover, there are neural

spikes that satisfied the thresholding and time-amplitude windowing criteria, but were not discriminated by the BMSI (SDO signal was not activated) as result of falling in the blanking periods, and were disregarded.

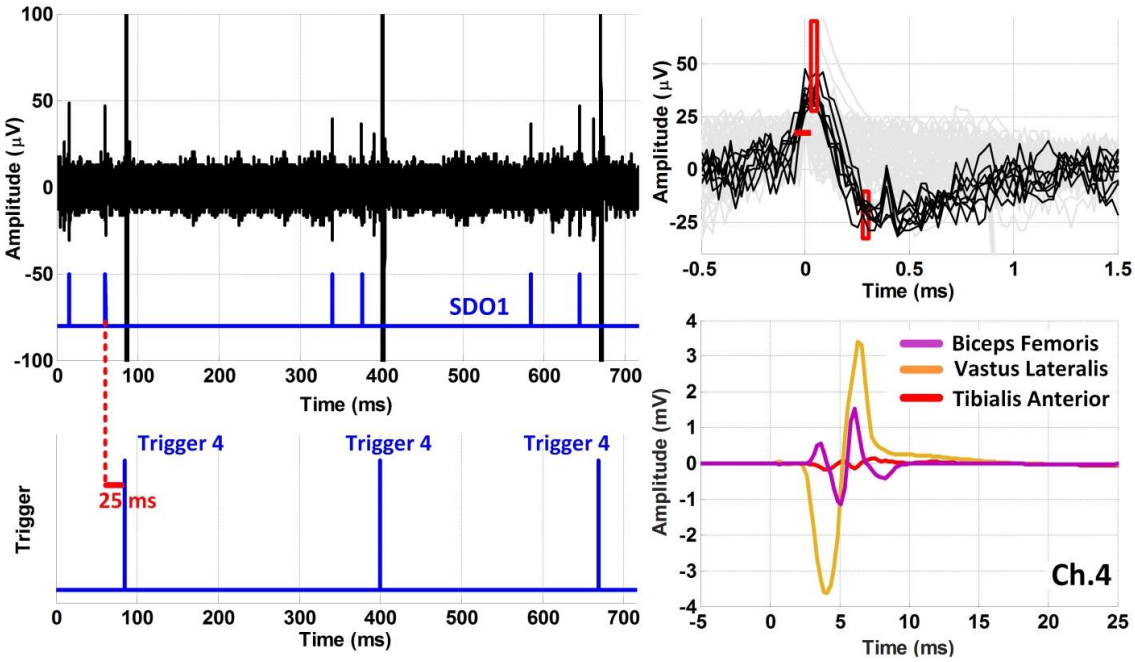

Figure 4.10: Closed-loop Individual ISMS on stimulating Ch.4 and resulted EMG signals; BMSI was stimulating Ch.4 after successful discrimination of two neural spikes on recording Ch.1.

4.4.2 Paired-Sequential ISMS

Fig. 4.11 depicts another experiment in which the BMSI was programmed to conduct paired sequential triggering after successful discrimination of three (N=3) neural spikes on recording Ch.1 within a time-bin duration of ~0.5s. In this scenario, spikes to stimulus delay was 20ms and the interchannel-delay between first two triggers (Triggers 1,2) and last two triggers (Triggers 3,4) was programmed to be 600ms. The BMSI was also set to deliver ISMS with a single monophasic current pulse (anodic, 10µA, 200µs) followed by passive discharge. In the top right plot, all the neural spikes that could satisfy the thresholding and time-amplitude windowing are shown (black) along with the neural

activities that were rejected (light grey.) EMG signals resulted from paired sequential stimulation are also shown in Fig. 4.11.

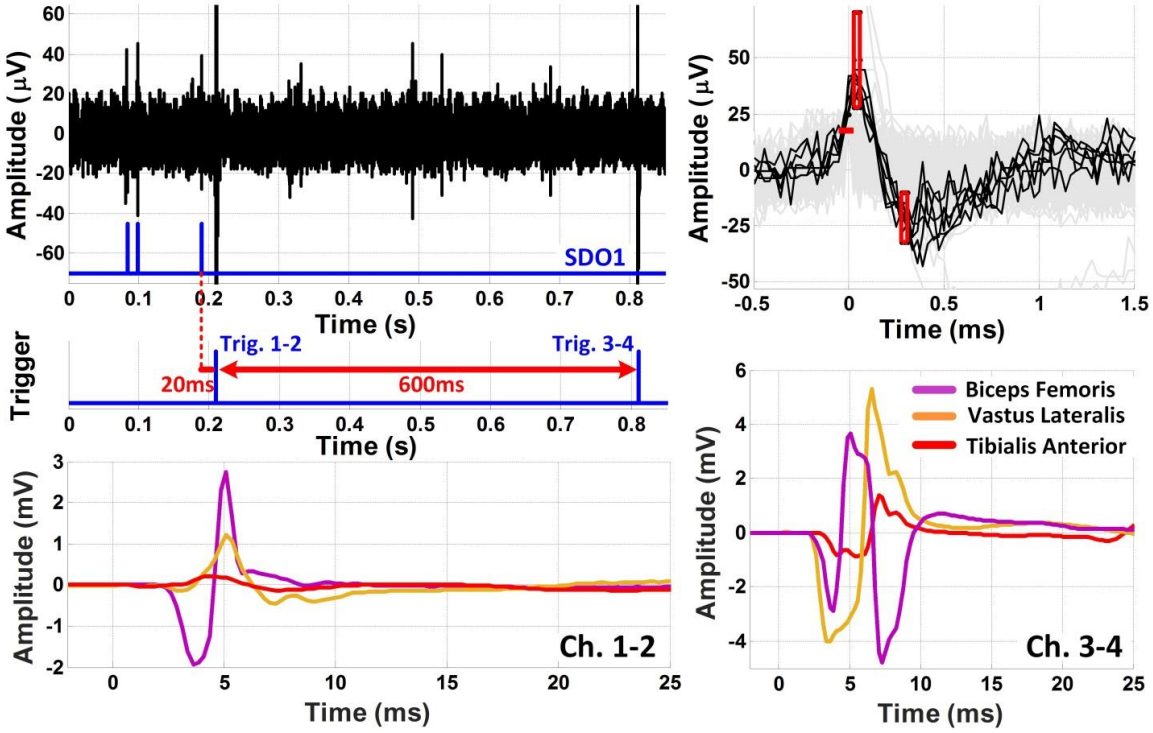

Figure 4.11: Closed-loop paired sequential ISMS; The BMSI was stimulating Ch.1,2 and Ch.3,4 with 600ms delay after successful discrimination of three neural spikes on recording Ch. 1.

4.4.3 Sequential ISMS

For the last scenario, Fig. 4.12 depicts EMG signals resulted from sequential, multichannel ISMS controlled by intracortical neural spikes and delivered to spinal cord below the injury level. Specifically, the BMSI was program to deliver single monophasic current pulse (anodic, 15μA, 200μs) followed by passive discharge when two neural spikes (N=2) could be discriminated within a 15ms window on neural recording channels 1 and 4 (CCO4 was defined as the logic AND operation of PASS1 and PASS4.) In this case, spike to stimulus delay was set to be 10ms and duration of PASS signals was 15ms. ISMS pulses were delivered to spinal cord of the rat with 220ms interchannel delay and

resulted the EMG signals shown in Fig. 4.12 (ISMS did not evoke considerable EMG activity on stimulating Ch. 1.)

Top left plots of Fig. 4.12, presents recorded neural data on recording Ch.1 and Ch. 4 along with the recorded SDO1, PASS1, SDO4, PASS4, and Triggers signals during the experiment. Besides, offline extracted neural spikes that could satisfy the thresholding and windowing criteria are shown. Again, it is worth mentioning that spikes that could satisfy the time amplitude windows are more than the few spikes that were discriminated by BMSI (activated SDO signals), because they were in the blanking periods and were disregarded. Hence, implemented blanking schemes provided a mechanism to prevent unwanted stimulus triggering during a period of stimulation.

Moreover, in Fig. 4.12, EMG signal patterns demonstrate distinct muscle pattern activation via multichannel ISMS in the SCI rat's spinal cord. ISMS activated the Biceps Femoris muscle consistently, activated Vastus Lateralis on two channels, and weakly activated Tibialis Anterior, indicating a specific muscle response at a precise location within the spinal cord. This demonstration of specificity suggests that it may be possible to achieve desirable muscle activation sequences by targeting ISMS to precise locations that can be identified through intraspinal mapping.

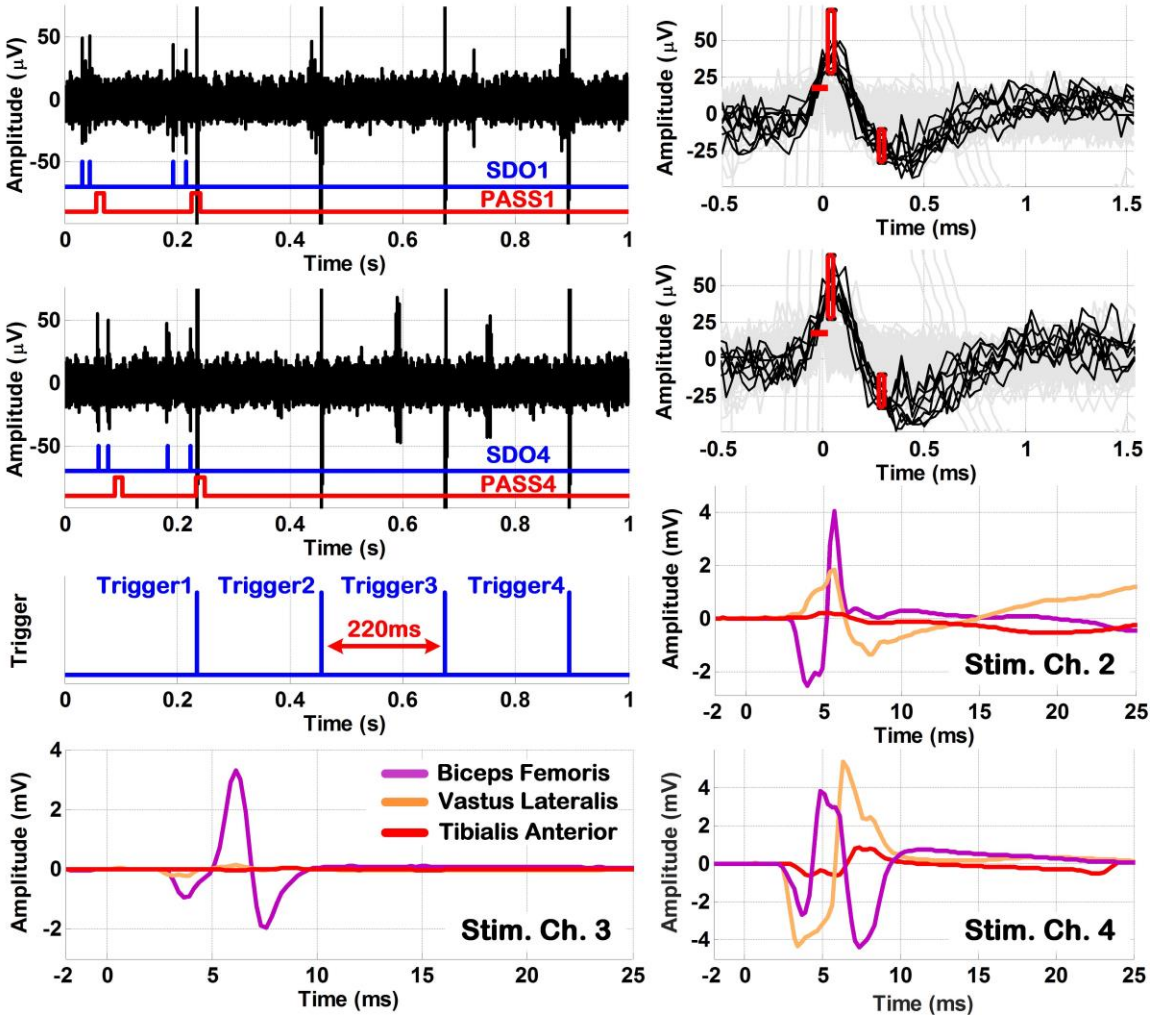

Figure 4.12: Closed-loop sequential ISMS; The BMSI was programmed to generate sequential ISMS when trigger-generation criteria were simultaneously satisfied on both Ch.1 and Ch. 4 (within a 15ms window), with sequential triggering criteria defined as the logic AND function of PASS1 and PASS4 signals.

4.5 References for Chapter 4

[4.1] S. Shahdoost, S. Frost, D. Guggenmos, C. Dunham, J. Borrell, S. Barbay, V. Tolosa, R. Nudo, and P. Mohseni "A Miniaturized Brain-Machine-Spinal Cord Interface for Closed-Loop Intraspinal Microstimulation" in 4th Minnesota Neuromodulation Symposium, April 14- 15, Minneapolis, MN, 2016. pp.105-105. http://neuromodulation.umn.edu/doc/MNS2016ProgramAndAbstracts.pdf

[4.2] S. Shahdoost, S. Frost, D. Guggenmos, C. Dunham, J. Borrell, S. Barbay, R. Nudo, and P. Mohseni, "A miniaturized brain-machine-spinal cord interface (BMSI) for closed-loop intraspinal microstimulation," 2016 IEEE Biomedical Circuits and Systems Conference (BioCAS), Shanghai, 2016, pp. 364-367.

[4.3] Azin, Meysam "A Battery-Powered Multichannel Microsystem for Activity-Dependent Intracortical Microstimulation." Electronic Thesis or Dissertation. Case Western Reserve University, 2011. https://etd.ohiolink.edu/

[4.4] R. E. Kass, U. Eden, E. Brown, *Analysis of Neural Data*. New York, NY: Springer, 2014.

[4.5] Alessandro Maccione, Mauro Gandolfo, Paolo Massobrio, Antonio Novellino, Sergio Martinoia, Michela Chiappalone, A novel algorithm for precise identification of spikes in extracellularly recorded neuronal signals, Journal of Neuroscience Methods, Volume 177, Issue 1, 15 February 2009, Pages 241-249.

Chapter 5

Conclusions, Contributions, and Future Work

Miniaturized brain machine body interfaces (BMBIs) form a new generation of implantable neuroprostheses that combine neural recording, signal processing, and microstimulation in a single device for closed-loop interfacing with the nervous system. Currently, most BMBIs operate in a so-called control-mode paradigm in which the user's intent to produce voluntary control of the user's own body is detected in cortical activity, and, after processing, activates the target to produce an action. Control-mode BMBIs are dealing with substantial challenges of designing optimal signal-processing and control algorithms, as well as efficient hardware realization, in particular in a miniaturized form, for real-time execution. Furthermore, they often require significant learning by the user, depending upon the complexity of the task, and need to be implanted throughout the user's lifetime, facing additional challenges related to long-term feasibility.

An alternative, conditioning-mode approach for BMBIs is based on mechanisms underlying neuroplasticity. The ability of the nervous system to alter the strength of

synaptic efficacy underlies learning and memory in healthy organisms, and is a mechanism for recovery after injury as well. Using the same cortical command signals of control-mode BMBIs, it is possible to condition neural connections that are remote from each other by timing the application of a small electrical pulse in the target region so that it occurs after a natural delay following cortical spike activity.

The main focus of this research work is to design and develop a miniaturized integrated neuromodulation microsystem *for the first time* that enables cortical control of intraspinal microstimulation to investigate the feasibility of functional recovery after spinal cord injury, in a conditioning mode paradigm. This has been accomplished in a three-step approach. In the first step, we developed a SoC, *SCI_Gen1* for robust multichannel intracortical neural recording and microstimulating *in vivo*. Next, in the second step, we developed an algorithm for generation of stimulus triggering from intracortical neural activity and implemented the proposed algorithm on an FPGA. *SCI_Gen1* and FPGA implementation of the algorithm has been interfaced and the functionality of the system was verified by conducting in vivo experiments. Finally, in the third step, we implemented a miniaturized SoC, *SCI_Gen2*, capable of multichannel intracortical neural recording, digital signal processing, and intraspinal microstimulation as a stand-alone BMSI for functional recovery after SCI.

5.1 Contributions

The major contributions of this research work to the field of biomedical microsystems are listed as follows

5.1.1 Design and Theory

- Understand the major performance limitations and tradeoffs involved in low-power design of integrated microsystems for biomedical applications.
- Obtain a fundamental knowledge of the system-level considerations to enable *combined* intracortical neural recording and electrical microstimulation on the same silicon substrate in highly integrated biomedical microsystems.
- Introduce a novel stimulus generation algorithm from intracortical spike activity and spike firing rate based on the basic principles of neuroplasticity for conditioning mode Brain-Machine-Body-Interfaces (BMBIs).

5.1.2 Development and Assembly

- Develop a multichannel neural recording and micro-stimulating SoC for simultaneous intracortical neural recording and intraspinal microstimulation.
- Develop a DSP unit on an FPGA device for the real-time generation of the stimulus triggering from intracortical neural activity.
- Develop a miniaturized, multichannel, battery-powered SoC as a Brain-Machine-Spinal cord Interface (BMSI) for closed-loop cortical control of intraspinal microstimulation.
- Develop associated peripheral hardware and software in conjunction with the BMSI system for conducting in vivo experiments in spinal cord injured laboratory rats.

5.1.3 Testing and Characterization

- Thorough benchtop testing and electrical performance characterization of the implemented and developed biomedical microsystems.
- Demonstration of combined single-chip, multichannel intracortical neural recording and intraspinal microstimulation in an anesthetized rat.
- First ever demonstration of on-the-fly stimulus generation from firing rate of intracortical spike activities for brain-machine-body interfaces (BMBI) in context of conditioning mode BMBIs.
- First ever demonstration of a miniaturized brain-machine-spinal cord interface (BMSI) for cortical control of intraspinal microstimulation.

5.2 Future Work

5.2.1 Increasing the Number of Recording and Stimulating Channels

In this PhD research, the goal was to develop a proof-of-concept BMSI for functional recovery in a rat model of SCI. For future applications, or animal/human models, an increased number of recording and/or stimulating channels might be required. The proposed DSP architecture in this design has a processing time of three clock cycle per channel, which with regard to 28 clock cycles for each ADC conversion; the same architecture can handle operation of up to 9 channels per module without any modifications. Besides, increasing the number of recording and stimulating channels will require higher power consumption and silicon area for the BMSI. Based on the area and power breakdown of the BMSI in previous chapter, an effective approach to reduce the

area and power simultaneously is to reduce SAR ADC resolution from 10 to 9 bits. The input-referred quantization noise of the SAR ADC ($\frac{V_{DD}}{\sqrt{12} \times Gain \times 2^{ENOB}}$) is ~0.8 μV_{rms} for a nominal gain of 60 dB which is less than input noise of LNA (~3 μV_{rms}). By reducing the number of bits from 10 to 9, not only reduces the power and area for ADC block, but also relaxes the current driving capability of the secondary amplifier (which with current condition is consuming ~18% of the total power) resulting in significant power and area savings [4.4].

5.2.2 Adaptive Spike Discriminators

In this work we presented a thresholding and time-amplitude windowing algorithm for discriminating spikes from existing noise/artifacts in the recorded intracortical neural activity. While a higher number of windows can certainly be used to impose more stringent criteria for spike discrimination, we have generally found two windows (along with thresholding) to suffice in our experimental recording sessions. This approach is computationally simple and can therefore be efficiently implemented in low-power, resource-constrained hardware, which is especially important when the number of input channels is ultimately increased for large-scale recording from cortical regions. Currently, the spike discrimination parameters are determined empirically by the user offline during test recording sessions prior to the actual experiment and programmed into the FPGA shift register. This *a priori* knowledge of the shape and other characteristics of the recorded spikes on multiple channels allows the user to not only select the most active channels as the source of stimulus trigger generation, but also to select the spike discrimination parameters in such a way that would maximize the number of

discriminated spikes and hence that of spike-stimulus pairs. The drawback of this approach is that user adjustment of thresholding and time-amplitude window parameters would be necessary in chronic experiments in response to changes in the position of recording sites and background noise level, as well as formation of glial scars, electrode drift, etc.

Table 5.1: Summary of CMOS-implemented Spike Detectors Performances

	[5.1]	**[5.2]**	**[5.3]**	**[5.4]**	**[5.5]**	**This work**
Technology (µm)	0.18	0.13	0.18	0.13	0.13	0.35
Power Supply (V)	1.8	1.2	1.8	1.2	1	1.5
Power/Ch. (µW)	0.78	85	1.5	1.7*	0.95	0.32
Area/Ch. (mm^2)	0.07	0.41	0.03	0.014	0.17	0.022
Detection method	MTEO	EC-PC	NEO	SWT	NEO	Threshold & windowing
Domain	Analog	Digital	Analog	Digital	Analog	Digital

*Simulation results

As an alternative, it is possible to use more computationally complex algorithms based on nonlinear energy operators (NEO), multi-resolution Teager energy operators (MTEO), or matched filters. Such algorithms could automatically extract optimal spike discrimination parameters based on the statistics of the input neural data and exhibit superior performance with regard to true- and false-positive rates at low input signal-to-noise ratios (SNR). Still, these approaches will need extra power and silicon area for the BMSI. In Table 5.1 power and area per channel for our algorithm is compared with other CMOS-implemented spike discriminators.

5.3 References for Chapter 5

[5.1] B. Gosselin and M. Sawan, “An ultra low-power CMOS automatic action potential detector,” IEEE Trans. Neural Syst. Rehabil. Eng., vol. 17, no. 4, pp. 346–353, Aug. 2009.

[5.2] Y. Zhou et al., “On the robustness of EC-PC spike detection method for online neural recording,” J. Neurosci. Methods, vol. 235, pp. 316–330, 2014.

[5.3] E. Koutsos, S. E. Paraskevopoulou, and T. G. Constandinou, “A 1.5 uW NEO-based spike detector with adaptive-threshold for calibrationfree multichannel neural interfaces,” in IEEE Int. Symp. Circuits Syst., 2013, pp. 1922–1925.

[5.4] Y. Yang, C. S. Boling, A. M. Kamboh and A. J. Mason, "Adaptive Threshold Neural Spike Detector Using Stationary Wavelet Transform in CMOS," in IEEE Transactions on Neural Systems and Rehabilitation Engineering, vol. 23, no. 6, pp. 946-955, Nov. 2015.

[5.5] J. Holleman, A. Mishra, C. Diorio and B. Otis, "A micro-power neural spike detector and feature extractor in .13µm CMOS," 2008 IEEE Custom Integrated Circuits Conference, San Jose, CA, 2008, pp. 333-336.

Dissertation Bibliography

[1.1] Christopher & Dana Reeve Foundation. Available online at www.christopherreeve.org.

[1.2] R. van den Brand, et al., "Restoring voluntary control of locomotion after paralyzing spinal cord injury," Science, vol. 336, pp. 1182-1185, June 1, 2012.

[1.3] Y. K. Lo, et al., "A 176-channel 0.5cm3 0.7g wireless implant for motor function recovery after spinal cord injury," in Dig. Tech. Papers IEEE Int. Solid-State Circuits Conf. (ISSCC'16), pp. 382-383, February 2016.

[1.4] L. R. Hochberg, et al., "Reach and grasp by people with tetraplegia using a neurally controlled robotic arm," Nature, vol. 485, pp. 372-375, May 2012.

[1.5] C. E. Bouton, et al., "Restoring cortical control of functional movement in a human with quadriplegia," Nature, vol. 533, pp. 247-250, May 2016.

[1.6] A. Jackson, J. Mavoori, and E. E. Fetz, "Long-term motor cortex plasticity induced by an electronic neural implant," Nature, vol. 444, pp. 56-60, 2006.

[1.7] D. J. Guggenmos, et al., "Restoration of function after brain damage using a neural prosthesis," Proc. Natl. Acad. Sci. USA (PNAS), vol. 110, no. 52, pp. 21177-21182, December 24, 2013.

[1.8] S. Stanslaski, et al., "Design and validation of a fully implantable, chronic, closed-loop neuromodulation device with concurrent sensing and stimulation," IEEE Trans. Neural Syst. Rehab. Eng., vol. 20, no. 4, pp. 410-421, July 2012.

[1.9] P. J. Grahn, et al., "Restoration of motor function following spinal cord injury via optimal control of intraspinal microstimulation: toward a next-generation closed-loop neural prosthesis," Front. Neurosci., vol. 8, no. 296, pp. 1-12, September 2014.

[1.10] C. T. Moritz, S. I. Perlmutter, and E. E. Fetz, "Direct control of paralyzed muscles by cortical neurons," Nature, vol. 456, pp. 639-643, 2008.

[1.11] J. B. Zimmermann and A. Jackson, "Closed-loop control of spinal cord stimulation to restore hand function after paralysis," Front. Neurosci., vol. 8, no. 87, pp. 1-8, May 2014.

[1.12] Mondello, S. E., Kasten, M. R., Horner, P. J., and Moritz, C. T., "Therapeutic intraspinal stimulation to generate activity and promote long-term recovery." Front. Neurosci. 8:21. doi: 10.3389/fnins.2014.00021, 2014.

[1.13] Mushahwar, V. K., and Horch, K. W. “Selective activation and graded recruit- ment of functional muscle groups through spinal cord stimulation.” Ann. N.Y. Acad. Sci. 860, 531–535, 1998.

[1.14] Mushahwar, V. K., Gillard, D. M., Gauthier, M. J., and Prochazka, A. “Intraspinal micro stimulation generates locomotor-like and feedback- controlled movements.” IEEE Trans. Neural Syst. Rehabil. Eng. 10, 68–81, 2002.

[1.15] Mushahwar, V. K., Aoyagi, Y., Stein, R. B., and Prochazka, A. “Movements generated by intraspinal microstimulation in the intermediate gray matter of the anesthetized, decerebrate, and spinal cat.” Can. J. Physiol. Pharmacol. 82, 702–714, 2004.

[1.16] Moritz, C. T., Lucas, T. H., Perlmutter, S. I., and Fetz, E. E. ”Forelimb movements and muscle responses evoked by microstimulation of cervical spinal cord in sedated monkeys.” J. Neurophysiol. 97, 110–120, 2007.

[1.17] Sunshine, M. D., Cho, F. S., Lockwood, D. R., Fechko, A. S., Kasten, M. R., and Moritz, C. T. “Cervical intraspinal microstimulation evokes robust forelimb movements before and after injury.” J. Neural Eng. 10:036001. doi: 10.1088/1741-2560/10/3/036001, 2013.

[1.18] Edgerton, V. R., and Harkema, S. “Epidural stimulation of the spinal cord in spinal cord injury: current status and future challenges. Expert Rev. Neurother. 11, 1351–1353. doi: 10.1586/ern.11.129, 2012.

[1.19] Van Den Brand, R., Heutschi, J., Barraud, Q., Digiovanna, J., Bartholdi, K., Huerlimann, M., et al. “Restoring voluntary control of locomotion after paralyzing spinal cord injury.” Science 336, 1182–1185. doi: 10.1126/sci- ence.1217416, 2012.

[1.20] Brus-Ramer, M., Carmel, J. B., Chakrabarty, S., and Martin, J. H. “Electrical stimulation of spared corticospinal axons augments connections with ipsi- lateral spinal motor circuits after injury.” J. Neurosci. 27, 13793–13801. doi: 10.1523/JNEUROSCI.3489-07, 2007.

[1.21] K. Abdelhalim, H. Mazhab Jafari, L. Kokarovtseva, J. L. P. Velazquez, and R. Genov, “64-channel UWB wireless neural vector analyzer SOC with a closed-loop phase synchrony-triggered neurostimulator,” IEEE J. Solid-State Circuits, vol. 48, no. 10, pp. 2494-2510, October 2013.

[1.22] T. L. Skarpaas and M. J. Morrell, “Intracranial stimulation therapy for epilepsy,” Neurotherapeutics, vol. 6, pp. 238-243, 2009.

[1.23] D. J. Guggenmos, M. Azin, S. Barbay, J. D. Mahnken, C. Dunham, P. Mohseni, and R. J. Nudo, “Restoration of function after brain damage using a neural prosthesis,” in Proc. Natl. Acad. Sci. USA, in press.

[1.24] M. Azin, D. J. Guggenmos, S. Barbay, R. J. Nudo, and P. Mohseni, “A battery-powered activity-dependent intracortical microstimulation IC for brain-machine-brain interface,” IEEE J. Solid-State Circuits, vol. 46, no. 4, pp. 731-745, April 2011.

[1.25] A. T. Avestruz, W. Santa, D. Carlson, R. Jensen, S. Stanslaski, A. Helfenstine, and T. Denison, “A 5μW/channel spectral analysis IC for chronic bidirectional brain-machine interfaces,” IEEE J. Solid-State Circuits, vol. 43, no. 12, pp. 3006-3024, December 2008.

[1.26] S. Stanslaski, P. Afshar, P. Cong, J. Giftakis, P. Stypulkowski, D. Carlson, D. Linde, D. Ullestad, A. T. Avestruz, and T. Denison, “Design and validation of a fully implantable, chronic, closed-loop neuromodulation device with concurrent sensing and stimulation,” IEEE Trans. Neural Syst. Rehab. Eng., vol. 20, no. 4, pp. 410-421, July 2012.

[1.27] Nishimura, Y., Perlmutter, S.I., & Fetz, E. E., “Restoration of upper limb movement via artificial corticospinal and musculospinal connections in a monkey with spinal cord injury.” Frontiers in neural circuits, 7, 2013.

[1.28] Nishimura Y, Perlmutter SI, Eaton RW, Fetz EE, “Spike-timing-dependent plasticity in primate corticospinal connections induced during free behavior.” Neuron 80(5):1301–1309, 2013.

[1.29] Zanos, S.; Richardson, A.G.; Shupe, L.; Miles, F.P.; Fetz, E.E., "The Neurochip-2: An Autonomous Head-Fixed Computer for Recording and Stimulating in Freely Behaving Monkeys," in Neural Systems and Rehabilitation Engineering, IEEE Transactions on , vol.19, no.4, pp.427-435, Aug. 2011.

[1.30] J. Mavoori et al., “An autonomous implantable computer for neural recording and stimulation in unrestrained primates,” J. Neurosci. Methods, vol. 148, no. 1, pp. 71–77, Oct. 2005.

[2.1] S. Shahdoost, S. Frost, R. Nudo, and P. Mohseni, “A multichannel corticospinal interface IC for intracortical spike recording and distinct muscle pattern activation via intraspinal microstimulation,” in *Proc. 57th Annu. Int. IEEE Midwest Symp. Circuits and Systems (MWSCAS’14)*, pp. 310-313, College Station, TX, August 3-6, 2014.

[2.2] S. Shahdoost, S. Frost, , G. Van Acker, S. DeJong, C. Dunham, S. Barbay, R. Nudo, and P. Mohseni “Towards a miniaturized brain-machine-spinal cord interface (BMSI) for restoration of function after SCI,” 41th Neural Interfaces Conference (NIC), June 23- 25, Dallas, Texas, 2014.

[2.3] M. Azin, D. J. Guggenmos, S. Barbay, R. J. Nudo, and P. Mohseni, “A battery-powered activity-dependent intracortical microstimulation IC for brain-machine-brain interface,” *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 731-745, April 2011.

[2.4] T. G. Constandinou, J. Georgiou, and C. Toumazou, “A partial-current-steering biphasic stimulation driver for vestibular prostheses,” *IEEE Trans. Biomed. Circuits and Systems*, vol. 2, no. 2, pp. 106-113, June 2008.

[2.5] X. Liu, A. Demosthenous, and N. Donaldson, “An integrated implantable stimulator that is fail-safe without off-chip blocking capacitors,” *IEEE Trans. Biomed. Circuits and Systems*, vol. 2, no. 3, pp. 231-244, September 2008.

[2.6] R. R. Harrison, “The design of integrated circuits to observe brain activity,” *Proceedings of the IEEE*, vol. 96, no. 7, pp. 1203-1216, July 2008.

[2.7] M. D. Scott, B. E. Boser, and K. S. J. Pister, “An ultralow-energy ADC for smart dust,” *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1123-1129, July 2003.

[2.8] M. Ghovanloo and K. Najafi, “A compact large-voltage-compliance high-output-impedance programmable current source for implantable microstimulators,” *IEEE Trans. Biomed. Eng.*, vol. 52, no. 1, pp. 97-105, January 2005.

[2.9] Y. Tsividis, *Operation and Modeling of the MOS Transistor*, 2nd ed., New York, NY: Oxford University Press, 1999.

[2.10] S. Guo, H. Lee, and P. Loizou, “A 9-bit configurable current source with enhanced output resistance for cochlear stimulators,” in *Proc. Custom Integrat. Circ. Conf. (CICC’08)*, pp. 511-514, September 2008.

[2.11] M. M. Ahmadi, “A new modeling and optimization of gain-boosted cascode amplifier for high-speed and low-voltage applications,” *IEEE Trans. Circuits and Systems-II*, vol. 53, no. 3, pp. 169-173, March 2006.

[3.1] S. Shahdoost *et al*., "Towards a miniaturized brain-machine-spinal cord interface (BMSI) for restoration of function after spinal cord injury," *2014 36th Annual International Conference of the IEEE Engineering in Medicine and Biology Society*, Chicago, IL, 2014, pp. 486-489.

[3.2] S. Shahdoost and P. Mohseni, "An FPGA platform for generation of stimulus triggering based on intracortical spike activity in brain-machine-body interface (BMBI) applications," *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, Lisbon, 2015, pp. 1766-1769.

[3.3] S. Shahdoost *et al*., "Cortical control of intraspinal microstimulation: Toward a new approach for restoration of function after spinal cord injury,"*2015 37th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*, Milan, 2015, pp. 2159-2162.

[3.4] Shahdoost, S.; Nudo, R.; Mohseni, P., "A brain-machine-spinal cord interface (BMSI) for functional recovery after spinal cord injury," in Student Research Preview Session (SRP), International Solid State Conf., ISSCC, San Francisco, CA, Feb. 2015.

[3.5] S. Shahdoost, R. J. Nudo and P. Mohseni, "Generation of Stimulus Triggering from Intracortical Spike Activity for Brain-Machine-Body-Interfaces (BMBIs)," in *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, vol. 25, no.7, pp. 998-1008, July 2017.

[4.1] S. Shahdoost, S. Frost, D. Guggenmos, C. Dunham, J. Borrell, S. Barbay, V. Tolosa, R. Nudo, and P. Mohseni “A Miniaturized Brain-Machine-Spinal Cord Interface for Closed-Loop Intraspinal Microstimulation” in 4th Minnesota Neuromodulation Symposium, April 14- 15, Minneapolis, MN, 2016. pp.105-105.
http://neuromodulation.umn.edu/doc/MNS2016ProgramAndAbstracts.pdf

[4.2] S. Shahdoost, S. Frost, D. Guggenmos, C. Dunham, J. Borrell, S. Barbay, R. Nudo, and P. Mohseni "A miniaturized Brain-Machine-Spinal Cord Interface (BMSI) for Closed-Loop Intraspinal Microstimulation," 2016 Biomedical Circuits and Systems Conference (BioCAS), Under Review.

[4.3] Azin, Meysam "A Battery-Powered Multichannel Microsystem for Activity-Dependent Intracortical Microstimulation." Electronic Thesis or Dissertation. Case Western Reserve University, 2011. https://etd.ohiolink.edu/

[4.4] R. E. Kass, U. Eden, E. Brown, *Analysis of Neural Data*. New York, NY: Springer, 2014.

[4.5] Alessandro Maccione, Mauro Gandolfo, Paolo Massobrio, Antonio Novellino, Sergio Martinoia, Michela Chiappalone, A novel algorithm for precise identification of spikes in extracellularly recorded neuronal signals, Journal of Neuroscience Methods, Volume 177, Issue 1, 15 February 2009, Pages 241-249.

[5.1] B. Gosselin and M. Sawan, "An ultra low-power CMOS automatic action potential detector," IEEE Trans. Neural Syst. Rehabil. Eng., vol. 17, no. 4, pp. 346–353, Aug. 2009.

[5.2] Y. Zhou et al., "On the robustness of EC-PC spike detection method for online neural recording," J. Neurosci. Methods, vol. 235, pp. 316–330, 2014.

[5.3] E. Koutsos, S. E. Paraskevopoulou, and T. G. Constandinou, "A 1.5 uW NEO-based spike detector with adaptive-threshold for calibrationfree multichannel neural interfaces," in IEEE Int. Symp. Circuits Syst., 2013, pp. 1922–1925.

[5.4] Y. Yang, C. S. Boling, A. M. Kamboh and A. J. Mason, "Adaptive Threshold Neural Spike Detector Using Stationary Wavelet Transform in CMOS," in IEEE Transactions on Neural Systems and Rehabilitation Engineering, vol. 23, no. 6, pp. 946-955, Nov. 2015.

[5.5] J. Holleman, A. Mishra, C. Diorio and B. Otis, "A micro-power neural spike detector and feature extractor in .13μm CMOS," 2008 IEEE Custom Integrated Circuits Conference, San Jose, CA, 2008, pp. 333-336.